

**2025 38th International
Conference on VLSI Design and
2024 23rd International
Conference on Embedded Systems
(VLSID 2025)**

**Bangalore, India
4-8 January 2025**



**IEEE Catalog Number: CFP25041-POD
ISBN: 979-8-3315-2245-2**

**Copyright © 2025 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP25041-POD
ISBN (Print-On-Demand):	979-8-3315-2245-2
ISBN (Online):	979-8-3315-2244-5
ISSN:	1063-9667

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2025 38th International Conference on VLSI Design and 2025 24th International Conference on Embedded Systems (VLSID) VLSID 2025

Table of Contents

Foreword	xvii
VLSI Design Conference History	xviii
Message from the Steering Committee Chair	xx
Message from the General Chairs	xxi
Message from the Technical Program Chairs	xxiv
Message from the IEEE Liaisons and Publication Chairs	xxv
Committees	xxvi
Technical Programme Committee	xxviii
Reviewers	xxix

2025 38th International Conference on VLSI Design and 2025 24th International Conference on Embedded Systems (VLSID)

MERGERS: Multi-Access Edge Resource GovErnance for Real-Time SaaS Systems	1
<i>Aakashjit Bhattacharya (Advanced Technology Development Centre, IIT Kharagpur, India), Arnab Sarkar (Advanced Technology Development Centre, IIT Kharagpur, India), and Ansuman Banerjee (Advanced Computing and Microelectronics Unit, ISI Kolkata, India)</i>	
PrOFraC: Property Ordering and Frame Clause Reuse for Multi-Property Verification	7
<i>Sourav Das (Indian Institute of Technology Kharagpur, India), Aritra Hazra (Indian Institute of Technology Kharagpur, India), Pallab Dasgupta (Synopsys Inc., USA), Himanshu Jain (Synopsys Inc., USA), and Sudipta Kundu (Synopsys Inc. USA)</i>	
Bidirectional Spiking Neuron Based Dual-Mode Signal Acquisition Front-End System	13
<i>Tamal Chowdhury (IIT Kharagpur, Kharagpur, India) and Pradip Mandal (IIT Kharagpur, Kharagpur, India)</i>	
Lichen: Leveraging Coupled Heterogeneity	19
<i>Prakhar Diwan (Indian Institute of Technology Bombay, India), Nirmal Kumar Boran (National Institute of Technology Calicut, India), and Virendra Singh (Indian Institute of Technology Bombay, India)</i>	

Physical Synthesis Optimization Prediction Using Machine Learning	25
<i>Sourav Saha (Intel India Pvt. Ltd., India), Anmol Khatri (Intel India Pvt. Ltd., India), Lalit Arora (Intel India Pvt. Ltd., India), Raj Yadav (Intel India Pvt. Ltd., India), and Rakshit Bazaz (Intel India Pvt. Ltd., India)</i>	
Enhancing Reliability and Energy Efficiency in Network-on-Chip Architectures Through Hybrid Sorting Algorithm-Based Core Mapping	31
<i>B Naresh Kumar Reddy (NIT Tiruchirappalli, India), Srinivasulu Jogi (NIT Tiruchirappalli, India), and Charan Krishna Y (NIT Tiruchirappalli, India)</i>	
True-PolyTronik: Securing Circuits Against Laser Logic State Imaging Attack Using RFET	37
<i>Sajjad Parvin (University of Bremen, Germany), Chandan Kumar Jha (University of Bremen, Germany), Frank Sill Torres (German Aerospace Center, Germany), and Rolf Drechsler (University of Bremen, Germany; DFKI GmbH, Germany)</i>	
FARAD: Automated Formal Verification of Approximate Restoring Array Dividers	43
<i>Chandan Kumar Jha (University of Bremen, Germany), Khushboo Qayyum (DFKI GmbH, Germany), Muhammad Hassan (University of Bremen, Germany; DFKI GmbH, Germany), and Rolf Drechsler (University of Bremen, Germany; DFKI GmbH, Germany)</i>	
CRIS-b: A High-Speed Unified Modulo Reduction Algorithm and Hardware Architecture for CRYSTALS-Kyber	49
<i>Rahul Shrestha (Indian Institute of Technology Mandi) and Alip Majumdar (Indian Institute of Technology Mandi)</i>	
hbcLock: Encrypted RF Communication Utilizing Body-Coupled Keys for the Internet of Bodies.	55
<i>Soumick Majumdar (International Institute of Information Technology, India), Anshul Madurwar (International Institute of Information Technology, India), Anmol Shetty (International Institute of Information Technology, India), and Kurian Polachan (International Institute of Information Technology, India)</i>	
FRoZN: Fault-Tolerant Routing Technique Using Reinforcement Learning for ZMesh NoC	61
<i>Jitesh Choudhary (CDAC India and Bits Pilani Hyderabad Campus, India), Imran Hussain Barbhuiya (CDAC INDIA, India), Dharrun Singh. M (CDAC INDIA, India), and Soumya J (BITS Pilani Hyderabad Campus, India)</i>	
Optimal Respiratory Rate Estimation with mmWave Sensing Using PYNQ System-on-Chip Platform.....	67
<i>Mohammed Musayyeb Sherwani (Aligarh Muslim University, India), Mohammad Abdul Azeem (R.G.U.K.T Basar, India), Mohd Usman (Aligarh Muslim University, India), Siddique Ahmad (Aligarh Muslim University, India), Mujeev Khan (Aligarh Muslim University, India), R Shamim (Aligarh Muslim University, India), and Mohd Wajid (Aligarh Muslim University, India)</i>	

HapticGuide: Interactive Wearable Braille Guide for Enhancing Visual Education	73
<i>Divyansh Singhal (International Institute of Information Technology Bangalore, India), Yash Gupta (International Institute of Information Technology Bangalore, India), Daksh Sharma (International Institute of Information Technology Bangalore, India), Chinmay Sultania (International Institute of Information Technology Bangalore, India), and Madhav Rao (International Institute of Information Technology Bangalore, India)</i>	
Interconnect Optimization for Timing and Power [IOTAP]	79
<i>Sourav Saha (Intel India Pvt. Ltd., India), Sagar Rana (Intel India Pvt. Ltd., India), Keshav Patil (Intel India Pvt. Ltd., India), and Nagamaheswar Harivelam Srinivas Gari (Intel India Pvt. Ltd., India)</i>	
A Study on Efficiency Improvements of DNN Accelerators via Denormalized Arithmetic Elimination	85
<i>Alexander Kharitonov (University of Stuttgart, Germany) and Sandip Kundu (University of Massachusetts, USA)</i>	
Optimizing Bandwidth Utilization Through Word Based Compression in Main Memories	91
<i>Aswathy N S (Indian Institute of Technology Guwahati), Harsh Verma (Indian Institute of Technology Guwahati), and Hemangee K. Kapoor (Indian Institute of Technology Guwahati)</i>	
Accelerating U-Net: A Patchwise Memory Optimization Approach for Image Segmentation	97
<i>Chaitanya Modiboyina (Indian Institute of Technology Kharagpur, India), Syam Babu Gundumilli (Google India private Limited, India), Soumya Kanti Ghosh (Indian Institute of Technology kharagpur, India), and Indrajit Chakrabarti (Indian Institute of Technology kharagpur, India)</i>	
Pin Efficient Tri-Level Based Inductive Coupling Transceiver for 3D ICs	103
<i>Soumojit Bakshi (IIT Bhubaneswar), V K Surya (IIT Bhubaneswar), and Nijwm Wary (IIT Bhubaneswar)</i>	
ABMF: Adaptive Bonsai Merkle Forests for Efficient Integrity Verification in Secure Persistent Memories	109
<i>Hemangee K Kapoor (Indian Institute of Technology Guwahati) and Kartikay Bhardwaj (Indian Institute of Technology Guwahati)</i>	
A 0.27-THz Frequency Multiplier Chain Using Harmonic Mixing with Multiplication of $\times 18$ in 65-nm CMOS	115
<i>Shiva Prasad Bollam (IIT Guwahati, India) and Mahima Arrawatia (IIT Guwahati, India)</i>	
NSGA-RM: NSGA-II Evolved Performance Optimized Non-Homogeneous Recursive Polynomial Multiplier Architectures	121
<i>Daksh Sharma (International Institute of Information Technology Bangalore, India), Vasanthi D R (International Institute of Information Technology Bangalore, India), Sanampudi Gopala Krishna Reddy (International Institute of Information Technology Bangalore, India), and Madhav Rao (International Institute of Information Technology Bangalore, India)</i>	

Optimizing Multipliers: An Energy-Efficient Design Using a Novel 3:2 Compressor	127
<i>Hemanth Krishna L (Indian Institute of Technology, Mandi), Sreehari Veeramachaneni (Sri Sivasubramaniya Nadar College of Engineering, Chennai), Srinivasu Bodapati (Indian Institute of Technology, Mandi), Bhaskara Rao Jammu (GVP College of Engineering, Visakhapatnam), and Noor Mahammad Sk (Indian Institute of Information Technology Design and Manufacturing, Kancheepuram)</i>	
TOGGLE6.0: A 4.8Gbps Next Generation Area and Power Efficient Transceiver for Flash Memory Interface	133
<i>Hari Vijay Venkatanarayanan (Samsung Foundry, India), Rustum Prasad Sahu (Samsung Foundry, India), Maheswara Alamuru (Samsung Foundry, India), Ergam Reddy Battini (Samsung Foundry, India), Syed Mohammed Haroon (Samsung Foundry, India), Saurav Suman (Samsung Foundry, India), Deepika Mallela (Samsung Foundry, India), Sanjeeb Kumar Ghosh (Samsung Foundry, India), and Billy Koo (Samsung Foundry, Korea)</i>	
SHAKTI: Securing Hardware IPs by Cascade Gated Multiplexer-Based Logic Obfuscation	139
<i>Jugal Gandhi (CSIR-Central Electronics Engineering Research Institute (CEERI), India; Academy of Scientific and Innovative Research (AcSIR), India; Academy of Scientific and Innovative Research (AcSIR), India), Nikhil Handa (Birla Institute of Technology and Science (BITS) Pilani, India), Abhay Nayak (Birla Institute of Technology and Science (BITS) Pilani, India), Diksha Shekhawat (CSIR-Central Electronics Engineering Research Institute (CEERI), India; Academy of Scientific and Innovative Research (AcSIR), India), M. Santosh (CSIR-Central Electronics Engineering Research Institute (CEERI), India; Academy of Scientific and Innovative Research (AcSIR), India), Jaya Dofe (California State University Fullerton, USA), and Jai Gopal Pandey (CSIR-Central Electronics Engineering Research Institute (CEERI), India; Academy of Scientific and Innovative Research (AcSIR), India)</i>	
An SRAM-Based Multi-Operand Architecture Implementing Multi-Bit Boolean Functions Using In-Memory Periphery Computing	145
<i>Dhayan Dhananjaya Senanayake (Indian Institute of Technology Roorkee), Priyanshu Tyagi (Indian Institute of Technology Roorkee), Sparsh Mittal (Indian Institute of Technology Roorkee), and Rekha Singhal (TCS Research)</i>	
Design of Manchester Carry Chain Hybrid Adder for MASH 1-1-1 Delta Sigma Modulator for Fractional-N Frequency Synthesizers	151
<i>Abhinav S (IIIT Hyderabad), Karthikeya Busam (IIIT Hyderabad), Ishan Acharyya (IIIT Hyderabad), Anushka Tripathi (IIIT Hyderabad), and Abhishek Srivastava (IIIT Hyderabad)</i>	
Boosting System-on-Chip Performance Through AI-Assisted Optimization Using Compositional Neural Networks	157
<i>Priyatam Roy (Intel Corporation, India) and Surinder Sood (ARM, United Kingdom)</i>	

BMC Engine Sequencing with Graph Neural Network Embeddings of Hardware Circuits	163
<i>Soumik Guha Roy (Indian Statistical Institute, India), Adriz Chanda (University of Calcutta, India), Prateek Ganguli (University of Calcutta, India), Sumana Ghosh (Indian Statistical Institute, India), Ansuman Banerjee (Indian Statistical Institute, India), Raj Kumar Gajavelly (IBM Systems, India), and Sudhakar Surendran (Texas Instruments, India)</i>	
A Constructive High-Speed Crypto-Mining Approach with Dual SHA-256 on an FPGA	169
<i>Velamala Pavan Kumar (Centre for Multi-Core Architecture Computation (C-MAC), Department of ECE, Koneru Lakshmaiah Education Foundation, India) and Aravindhyan Alagarsamy (Centre for Multi-Core Architecture Computation (C-MAC), Department of ECE, Koneru Lakshmaiah Education Foundation, India)</i>	
A Wide Dynamic Range Differential Drive CMOS Rectifier for μ Watts RF Energy Harvesting Systems	175
<i>Chaya Hegde (IIT Dharwad, India), Arun Mohan (IIT Guwahati, India), Saroj Mondal (IIT Dharwad, India), and Roy P. Paily (IIT Guwahati, India)</i>	
A 0.75mm ² 407 μ W Real-Time Speech Audio Denoiser with Quantized Cascaded Redundant Convolutional Encoder-Decoder for Wearable IoT Devices	180
<i>Dimple Vijay Kochar (Massachusetts Institute of Technology, USA), Maitreyi Ashok (Massachusetts Institute of Technology, USA), and Anantha P. Chandrakasan (Massachusetts Institute of Technology, USA)</i>	
N-Well Patterning of p-Type CMOS Substrate for Improving Quality Factor of On-Chip Inductors at Millimeter-Wave Frequencies	186
<i>Subbareddy Chavva (Indian Institute of Space Science and Technology, India) and Immanuel Raja (Indian Institute of Space Science and Technology, India)</i>	
Serialized Control Interface ASIC for Distributed Controllers of Space-Borne RADAR	191
<i>Chiragkumar B. Patel (Space Applications Centre, Indian Space Research Organisation, India), Ajay Kumar Singh (Space Applications Centre, Indian Space Research Organisation, India), Himanshu N. Patel (Space Applications Centre, Indian Space Research Organisation, India), and Saravana Kumar Balasundaram (Space Applications Centre, Indian Space Research Organisation, India)</i>	
DuRTL - Information Flow Analysis Tool for Register Transfer Level Hardware Designs	197
<i>Lutz Schammer (Hamburg University of Technology, Germany), Gianluca Martino (Hamburg University of Technology, Germany), and Goerschwin Fey (Hamburg University of Technology, Germany)</i>	
An Innovative Solution to Improve Ultra Low Voltage Writability and Leakage in GPU SRAMs ..	203
<i>Deepesh Gujjar (MediaTek Bangalore Private Limited, India), Sanatkumar Upadhye (Mediatek Bangalore Pvt. Ltd., India), Sandipan Sinha (Mediatek Bangalore Pvt. Ltd., India), Taha Khursheed (Mediatek Bangalore Pvt. Ltd., India), Jigar Patel (Mediatek Bangalore Pvt. Ltd., India), Jaswinder Sidhu (Mediatek Bangalore Pvt. Ltd., India), Manish Trivedi (Mediatek Bangalore Pvt. Ltd., India), and Sagar Abachi (Mediatek Bangalore Pvt. Ltd., India)</i>	

Hardware Implementation of Blind Decoding of Downlink Control Information for 5G	208
<i>Anu Rajarajeswari Y (Centre of Excellence in Wireless Technology (CEWiT) IIT Madras, India), Nitin Chandrachoodan (Indian Institute of Technology Madras, India), Anji Babu Vadapalli (Centre of Excellence in Wireless Technology (CEWiT) IIT Madras, India), and Klutto Milleth J (Centre of Excellence in Wireless Technology (CEWiT) IIT Madras, India)</i>	
Startup Circuit For Relaxation Oscillators With Low Functional Current And Minimal Area	214
<i>Anubhav Srivastava (NXP Semiconductors Pvt Ltd, India), Sadique Mohammad Iqbal (NXP Semiconductors Pvt Ltd, India), Divya Tripathi (NXP Semiconductors Pvt Ltd, India), and Saurabh Goyal (NXP Semiconductors Pvt Ltd, India)</i>	
Effective Memory Management and Sparse Aware Cache for Row-Wise Sparse CNNs	219
<i>Balasubramaniam MC (Indian Institute Of Technology Madras, India), Basava Naga Girish Koneru (Indian Institute Of Technology Madras, India), and Nitin Chandrachoodan (Indian Institute Of Technology Madras, India)</i>	
FPUGen: A FrameWork to Generate Custom Floating Point FMA Accelerators on FPGAs	225
<i>Himanshu Kumar Rai (International Institute of Information Technology, India), Aishwarya Sridhar (Infineon Technologies Semiconductor India Pvt. Ltd.), Wolfgang Ecker (Infineon Technologies AG, Neubiberg, Bavaria, Germany), and Nanditha Rao (International Institute of Information Technology, India)</i>	
Advancing Rehabilitation Through Low Weight Hand Assistive System: Design and Impact Analysis	231
<i>Kushagra Singh (International Institute of Information Technology Bangalore, India), Kafil Abbas Momin (International Institute of Information Technology Bangalore, India), Anshul V Patil (International Institute of Information Technology Bangalore, India), and Madhav Rao (International Institute of Information Technology Bangalore, India)</i>	
Advancing Neural Network Performance with Probabilistic Computing for ReLU Function	237
<i>Amit Singh (IIT Mandi, India), Amit Kumar Jangid (IIT Mandi, India), and Srinivasu Bodapati (IIT Mandi, India)</i>	
E-DOSA: Efficient Dataflow for Optimising SNN Acceleration	243
<i>Hemangee K Kapoor (Indian Institute of Technology Guwahati, India), Imlijungla Longchar (Indian Institute of Technology Guwahati, India), and Binayak Behera (Indian Institute of Technology Guwahati, India)</i>	
Layer-Specific Hardware Pooling Designs for CNN Accelerators	249
<i>Vinay Rayapati (IIIT Bangalore, India), Mahati Basavaraju (IIIT Bangalore, India), and Madhav Rao (IIIT Bangalore, India)</i>	
TCAD Based Study of String Current Variability in 3D NAND Flash Memory	255
<i>Mrinmoy Mahapatra (Indian Institute of Technology Bhubaneswar, India), Prathamesh Ganesh Kekarjawlekar (Indian Institute of Technology Bhubaneswar, India), and Akshay K. (Indian Institute of Technology Bhubaneswar, India)</i>	

Early Bug Detector – A Verification Methodology for DFD-SoC RTL Parameters	261
<i>Bhagyalakshmi C (Intel Technologies Private Limited, India), Madhav Lekkala (Intel Technologies Private Limited, India), and Maneesh Pandey (Intel Technologies Private Limited, India)</i>	
PAF-Enc: Position Affine Encoding to Reduce bit-Flips in Non-Volatile Main Memories	266
<i>Swati Upadhyay (Indian Institute of Technology Guwahati, India) and Hemangee K. Kapoor (Indian Institute of Technology Guwahati, India)</i>	
A Tug-of-War Between Static and Dynamic Memory in Intel SGX	272
<i>Sandeep Kumar (IIT Delhi, India), Abhisek Panda (IIT Delhi, India), Advait Nerlikar (BITS Pilani, India), and Smruti R. Sarangi (IIT Delhi, India)</i>	
Multi-Object Detection Through Meta-Training in Resource-Constrained UAV-Based Surveillance Applications	278
<i>Abhishek Yadav (IIT-Jodhpur Rajasthan, India), Vyom Kumar Gupta (IIIT-ALLAHABAD, India), Kethireddy Harshith Reddy (IIT-Jodhpur Rajasthan, India), Masahiro Fujita (University of Tokyo, Japan), and Binod Kumar (IIT-Jodhpur Rajasthan, India)</i>	
Tunnel Magnetoresistance in Strained L10-FeAu Perpendicular Magnetic Tunnel Junction	284
<i>Rouf Rahman Sheikh (Indraprastha Institute of information Technology Delhi, India) and Ram Krishna Ghosh (Indraprastha Institute of Information Technology Delhi, India)</i>	
AI-Driven Anomaly Detection in Oscilloscope Images for Post-Silicon Validation	290
<i>Kowshic A. Akash (NXP Semiconductors, Hamburg, Germany), Tobias Wulf (NXP Semiconductors, Hamburg, Germany), Torsten Valentin (NXP Semiconductors, Hamburg, Germany), Alexander Geist (NXP Semiconductors, Hamburg, Germany), Ulf Kulau (Hamburg University of Technology, Germany), and Sohan Lal (Hamburg University of Technology, Germany)</i>	
QualiTi: Quantum Machine Learning Hardware Selection for Inferencing with Top-Tier Performance	296
<i>Koustubh Phalak (Pennsylvania State University) and Swaroop Ghosh (Pennsylvania State University)</i>	
8GHz Multi-Phase Ring VCO Design with Wide Tuning Range for SerDes Applications in 6nm FinFET Process	302
<i>Ravuru Vasudeva Reddy (Microchip Technology India Pvt. Ltd, India), Siva Kumar Rapina (Microchip Technology India Pvt. Ltd, India), Siddhartha Hazra (Microchip Technology India Pvt. Ltd, India), and K Sarangam (National Institute of Technology, India)</i>	
PPA-Aware Power Grid Optimization Techniques for Congested High Frequency Datapath Designs.....	308
<i>Cheryl Mary Joyce (Intel Technology India Pvt. Ltd., India), Parag Upadhyay (Intel Technology India Pvt. Ltd., India), Sashank Nishad (Intel Technology India Pvt. Ltd., India), and Abhimanyu Kakkur (Intel Technology India Pvt. Ltd., India)</i>	
DNA-CIM: DNA Sequence Analysis Using RRAM-Based Compute In-Memory Accelerator	314
<i>Chithambara Moorthii (Indian Institute of Technology - Delhi, India), Anmol Singla (National Institute of Technology, India), and Manan Suri (Indian Institute of Technology - Delhi, India)</i>	

K Band High Power Broadband AlGaIn/GaN HEMT Balanced Power Amplifier for Satellite Transponder	320
<i>Ritan Das (Indian Institute of Space Science and Technology, India) and Basudev Majumder (Indian Institute of Space Science and Technology, India)</i>	
Meta-Heuristic Optimization of Custom Heterogeneous Blocks Defined eFPGA Design	326
<i>Bhargav DV (International Institute of Information Technology-Bangalore, India), Pradyumna G (International Institute of Information Technology-Bangalore, India), and Madhav Rao (International Institute of Information Technology-Bangalore, India)</i>	
Accelerated Design Verification Coverage Closure Using Machine Learning	332
<i>Shivani Jayakumar (Texas Instruments), Prasanth Viswanathan Pillai (Texas Instruments), and Sumit Kumar Mandal (Indian Institute of Science)</i>	
Low Form-Factor Switchless Dual-Band Matching Network for RF Power Harvesting Systems ..	338
<i>Arun Mohan (Indian Institute of Technology, India), Saroj Mondal (Indian Institute of Technology, India), Yash N Rayudu (Birla Institute of Technology and Science Pilani, India), and Roy P. Paily (Indian Institute of Technology, India)</i>	
Physical Insights into the Leakage Mechanisms Governing the Scaling Trends in 4H-SiC Based Junctionless FETs	344
<i>Jaspreet Singh (IIT Delhi, India), Aakash Kumar Jain (IIT Delhi, India), and M. Jagadesh Kumar (IIT Delhi, India)</i>	
Constructing Rectilinear Steiner Minimum Tree with Conditional Generative Adversarial Network	351
<i>Kritanta Saha (Sister Nivedita University, India), Pritha Banerjee (University of Calcutta, India), and Susmita Sur-Kolay (Indian Statistical Institute, India)</i>	
CMOSP18 FD-SOI Technology Based MCU Achieving High Performance of 1.2GHz Using High Speed, Optimized Leakage & High Density Tightly Coupled Memory (TCM)	357
<i>Praveen Verma (STMicroelectronics Pvt. Ltd, India), Anuj Dhillon (STMicroelectronics Pvt. Ltd., India), Ashfaq Ahmed (STMicroelectronics Pvt. Ltd., India), Yagnesh VADERIYA (STMicroelectronics Pvt. Ltd., India), Chandan Singh (STMicroelectronics Pvt. Ltd., India), Veenita Kumari (STMicroelectronics Pvt. Ltd., India), and Harshit Sharma (STMicroelectronics Pvt. Ltd., India)</i>	
Low-Power and Superior Performance Design of Ternary Logic Cells Using CNFET and MOSFET Devices for VLSI Applications	362
<i>Siva Chinmai Varma Bhupathiraju (Mahindra University, India), Sridhara Sai Krishna (Mahindra University, India), Yashwanth Komuravelly (Mahindra University, India), and Ramakant Yadav (Mahindra University, India)</i>	
TIPAngle: Traffic Tracking at City Scale by Pose Estimation of Pan and Tilt Intersection Cameras	368
<i>Shreehari Jagadeesha (SCAI, Arizona State University), Edward Andert (SCAI, Arizona State University), and Aviral Shrivastava (SCAI, Arizona State University)</i>	

Symmetry-Based Synthesis For Interpretable Boolean Evaluation	374
<i>Andrea Costamagna (EPFL, Switzerland), Alan Mishchenko (UC Berkeley, USA), Satrajit Chatterjee (Kepler AI, USA), and Giovanni De Micheli (EPFL, Switzerland)</i>	
A Low-Power, Low-Noise, High-Performance Re-Convergent Clock Mesh Design for Large AI Compute Clusters	380
<i>Harivinay Kancharla (SiMa.ai, India) and Sounil Biswas (SiMa.ai, USA)</i>	
Analysis and Design Considerations for MASH of Noise Shaped SAR ADCs	386
<i>R Arundepakvel (Indian Institute of Technology, India) and Ankesh Jain (Indian Institute of Technology, India)</i>	
A Study on the Impact of Temperature-Dependent Ferroelectric Switching Behavior in 3D Memory Architecture	392
<i>Varun Darshana Parekh (The Pennsylvania State University, USA), Yi Xiao (The Pennsylvania State University, USA), Yixin Xu (The Pennsylvania State University, USA), Zijian Zhao (University of Notre Dame, USA), Zhouhang Jiang (University of Notre Dame, USA), Rudra Biswas (The Pennsylvania State University, USA), Sumitha George (North Dakota State University, USA), Kai Ni (University of Notre Dame, USA), and Vijaykrishnan Narayanan (The Pennsylvania State University, USA)</i>	
Atrial Flutter Detection System by AdEx Encoded Lead-II ECG	398
<i>Sushmi R (Indian Institute of Information Technology Design and Manufacturing, India), Priya K (Indian Institute of Information Technology Design and Manufacturing, India), and Binsu J. Kailath (Indian Institute of Information Technology Design and Manufacturing, India)</i>	
Codesign for Broadcast Addressing Biochip Towards Tamper-Resistance and Enhanced Reliability	404
<i>Ritwika Majumdar (University of Calcutta, India), Piyali Datta (Institute of Engineering & Management, University of Engineering and Management, India), Arpan Chakraborty (University of Calcutta, India; Inside S&R, India), and Rajat Kumar Pal (University of Calcutta, India)</i>	
Advancing Functional Safety: Improving Failure Mode Analysis and Fault Injection Using Automation and GNN Algorithms	410
<i>Amurt Prakash (Texas Instruments, India), Abhijeet Singh (Texas Instruments, India), Pooja Madhusoodhanan (Texas Instruments, India), Padma Arvind (Texas Instruments, India), Prasanth Viswanathan Pillai (Texas Instruments, India), Sanjay Das (University of Texas at Dallas, USA), and Kanad Basu (University of Texas at Dallas, USA)</i>	
Quantum Analysis of LESCA	416
<i>Sumanta Chakraborty (Techno International New Town, India), Debajyoti Mandal (Indian Institute of Information Technology Kalyani, India), and SK Hafizul Islam (Indian Institute of Information Technology Kalyani, India)</i>	
2D Thermal Contour Modeling of 14 nm SOI FinFET Using Machine Learning for Efficient Thermal Profile Prediction	421
<i>Banit Negi (NIT Uttarakhand, India), Hariharan Muthusamy (NIT Uttarakhand, India), and Vivek Kumar (NIT Uttarakhand, India)</i>	

An Efficient RISC-V Vector Coprocessor for Heart Rate Variability Detection on Edge	427
<i>Uday Kiran Pedada (NIT Kurukshetra, India), Tarun Sharma (IIIT Delhi, India), Deepank Grover (IIIT Delhi, India), and Sujay Deb (IIIT Delhi, India)</i>	
Fast Bit-Sliced VLSI Architectures on FPGA for Montgomery Domain Modular Inversion	433
<i>Soham Adhikary (Indian Institute of Technology Bhubaneswar, India) and Ayan Palchaudhuri (Indian Institute of Technology Bhubaneswar, India)</i>	
An Ensemble MLP-RF Model for the Prediction of DG-MOSFETs: Addressing Fabrication Process Variations	439
<i>Vaikunth Muthuraman (Anna University, India), Khushwant Sehra (University of Delhi, India), Vandana Kumari (University of Delhi, India), and Manoj Saxena (University of Delhi, India)</i>	
LO-SC: Local-Only Split Computing for Accurate Deep Learning on Edge Devices	445
<i>Lugi Capogrosso (University of Verona, Italy), Enrico Fraccaroli (University of Verona, Italy), Marco Cristani (University of Verona, Italy), Franco Fummi (University of Verona, Italy), and Samarjit Chakraborty (University of North Carolina at Chapel Hill, USA)</i>	
OwlsEye: Real-Time Low-Light Video Instance Segmentation on Edge and Exploration of Fixed-Posit Quantization	451
<i>Gaurav Shah (Indian Institute of Technology Gandhinagar), Abhinav Goud (Indian Institute of Technology Gandhinagar), Zaqi Momin (Indian Institute of Technology Gandhinagar), and Joycee Mekie (Indian Institute of Technology Gandhinagar)</i>	
Novel Hardware Architectures for PRESENT Block Cipher and its FPGA Realizations	457
<i>Ruby Mishra (Kalinga Institute of Industrial Technology, India), Manish Okade (National Institute of Technology, India), and Kamalakanta Mahapatra (National Institute of Technology, India)</i>	
HyCMAx: Power-Efficient Hybrid CMOS-Memristor Based Approximate Dividers for Error-Resilient Applications	463
<i>Monika Pokharia (Indian Institute of Technology, Gandhinagar), Het Trivedi (Indian Institute of Technology, Gandhinagar), Siddharth Doshi (Indian Institute of Technology, Gandhinagar), Ravi Hegde (Indian Institute of Technology, Gandhinagar), and Joycee Mekie (Indian Institute of Technology, Gandhinagar)</i>	
TRANSPose: Circuit Transformations for Power Side-Channel Security at Register Transfer Level	469
<i>Nilotpola Sarma (Indian Institute of Technology, Guwahati), Anuj Singh Thakur (Indian Institute of Technology, Guwahati), and Chandan Karfa (Indian Institute of Technology, Guwahati)</i>	
Optimization of Sub-Threshold Standard Cells for Energy Efficient Designs	475
<i>Vardhan Suroshi (PES University, India), Karthik B K (InCore Semiconductors, India), Vikram Kannur (PES University, India), Vinay Reddy (PES University, India), and Madhura Purnaprajna (PES University, India)</i>	
RISC-V Based Secure Processor Architecture for Return Address Protection	481
<i>Lalit Sharma (Indian Institute of Technology, India) and Neeraj Goel (Indian Institute of Technology, India)</i>	

A 0.5pJ/bit 7.2Gbps HBM3 PHY on Intel4 with EMIB Packaging and Unmatched Receiver Architecture on PHY Side with Per Bit Deskew Correction	487
<i>Aakash Hasnmukhray Mehta (Intel, India), Javed S Gaggatur (Intel, India), Mohammad M Rashid (Intel, USA), Sampath Dakshinamurthy (Intel, India), Aruna Kumar Lakya Srinivasamurthy (Intel, USA), Anil Kumar Goyal (Intel, India), Subbarao Manam (Intel, India), Harshit Gupta (Intel, India), Sandeep Sukumar (Intel, India), Vipin K Mishra (Intel, India), Koushik N S (Intel, India), Santosh Nekkanti (Intel, India), Sambaran Mitra (Intel, India), Pooja K Jadhav (Intel, India), Miryala Chandra Shekar (Intel, India), Dudekula Humayun (Intel, India), Michael C Rifani (Intel, USA), Jianyong Xie (Intel, USA), and Andrew P Collins (Intel, USA)</i>	
Leveraging Dual Output LUTs with Pipelining for Efficient BCD to Binary Converter on FPGA ...	493
<i>Santosh Kumar (Indian Institute of Technology, India) and Ayan Palchadhuri (Indian Institute of Technology, India)</i>	
A First-Principles-Based Comparative Study Between Pristine and Au-Modified Graphene Nanosheet Towards Acetaldehyde Sensing Performance	499
<i>Indranil Maity (Institute of Engineering and Management, India), Soubarno Chatterjee (Institute of Engineering and Management, India), and Souvik Bhanja (Institute of Engineering and Management, India)</i>	
Robust Verification Methodology for Scan Chain in Memories	505
<i>Rajat Kohli (NXP India Pvt. Ltd., India), Umang Deep (NXP India Pvt. Ltd., India), Vaishnavi Holla (NXP India Pvt. Ltd., India), and Jwalant Kumar Mishra (NXP India Pvt. Ltd., India)</i>	
Reliable High-Performance Programmable Voltage Regulator with 0.55A Sink Current for Cryo-Cooler Electronics in 0.18 μ m HV-CMOS Technology	510
<i>Nishant Kumar (Indian Institute of Technology, Gandhinagar), Hari Shanker Gupta (Space Applications Centre (ISRO)), and Nihar Ranjan Mohapatra (Indian Institute of Technology, Gandhinagar)</i>	
TimeFloats: Train-in-Memory with Time-Domain Floating-Point Scalar Products	516
<i>Maeesha Binte Hashem (University of Illinois at Chicago (UIC), USA), Benjamin Parpillon (University of Illinois at Chicago (UIC), USA; Fermi National Accelerator Lab (FNAL), USA), Dinithi Jayasuriya (University of Illinois at Chicago (UIC), USA), Divake Kumar (University of Illinois at Chicago (UIC), USA), and Amit Ranjan Trivedi (University of Illinois at Chicago (UIC), USA)</i>	
Efficient Mitigation of DRAM Row Buffer Conflict Using Request Clustering in Manycore Systems	522
<i>K Chitra (IIT Guwahati), Arjun Dey (IIT Guwahati), and Aryabartta Sahu (IIT Guwahati)</i>	
A Fully Autonomous 1.2A Auxiliary Buck DC-DC Converter for Fast Transient Load-on-Demand	528
<i>Shivam Agarwal (Indian Institute of Technology, Madras), Sivasai Guddanti (Indian Institute of Technology, Madras), and Qadeer A. Khan (Indian Institute of Technology, Madras)</i>	
MAGIC-Based High-Speed Adders for In-Memory Computing Using Memristors	534
<i>Shri Janani Senthil (Indian Institute of Technology, India) and Srinivasu B. (Indian Institute of Technology, India)</i>	

Unguided Machine Learning-Based Computation Offloading for Near-Memory Processing	540
<i>Satanu Maity (Indian Institute of Information Technology, India), Manojit Ghose (Indian Institute of Information Technology, India), Avinash Kumar (Indian Institute of Information Technology, India), Anol Chakraborty (Jorhat Engineering College, India), and Ankit Chakraborty (Jorhat Engineering College, India)</i>	
LAMA: A Latency Minimum Resource Constraint Accelerator for CNN Models	546
<i>Sutirtha Bhattacharyya (IACS Kolkata), Fedrick Nongpoh (Nagaland University), Karthik Maddala (Indian Institute of Technology Guwahati), E. Bhawani Eswar Reddy (Indian Institute of Technology Guwahati), and Chandan Karfa (Indian Institute of Technology Guwahati)</i>	
Precision Clock Generation with Reference Clock Loss Tolerant Dynamic Tuning to Enable Crystal Less SSD	552
<i>Pikul Sarkar (Western Digital, India), Nitin Gupta (Signitude, India), Pallat Aravind (Western Digital, India), Bhavin Odedara (Western Digital, India), and Dror Shahar (Western Digital, Israel)</i>	
Investigating Impact of Bit-Flip Errors in Control Electronics on Quantum Computation	558
<i>Subrata Das (Pennsylvania State University, USA), Avimita Chatterjee (Pennsylvania State University, USA), and Swaroop Ghosh (Pennsylvania State University, USA)</i>	
Enhancing Digital Microfluidic Biochip Operations with Scheduling Interval Method	564
<i>Nirmala N (Thiagarajar College of Engineering, India) and Gracia Nirmala Rani D (Thiagarajar College of Engineering, India)</i>	
An Experimental Demonstration of Neuronal Somatic Behavior Using 2D SnS Memristive Switching Characteristics and its Equivalent Circuit for Spiking Neural Network	569
<i>Anshul Awasthi (Birla Institute of Technology and Science (BITS) Pilani, India), Soumi Saha (Birla Institute of Technology and Science (BITS) Pilani, India), Parikshit Sahatiya (Birla Institute of Technology and Science (BITS) Pilani, India), and Surya Shankar Dan (Birla Institute of Technology and Science (BITS) Pilani, India)</i>	
A 14-nm Energy-Efficient and Reconfigurable Analog Current-Domain In-Memory Compute SRAM Accelerator	575
<i>Aya G. Amer (Massachusetts Institute of Technology, USA), Maitreyi Ashok (Massachusetts Institute of Technology, USA), Xin Zhang (IBM T. J. Watson Research Center, USA; MIT-IBM Watson AI Lab, USA), John Cohn (MIT-IBM Watson AI Lab, USA), and Anantha P. Chandrakasan (Massachusetts Institute of Technology, USA)</i>	
Author Index	581