2024 IEEE 33rd Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS 2024)

Toronto, Ontario, Canada
6-9 October 2024

IEEE Catalog Number:	**CFP24EPP-POD**
ISBN:	**979-8-3503-5124-8**

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24EPP-POD
ISBN (Print-On-Demand):	979-8-3503-5124-8
ISBN (Online):	979-8-3503-5123-1
ISSN:	2165-4107

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

Optimizing Power and Power Delivery for Data Center GPUs 1
Tawfik Rahal-Arabi, Paul Van Der Arend, Ashish Jain, Mehdi Saidi, Rashad Oreifej, Sriram Sundaram, Rajit Seahra

Electrothermal Co-Design Modeling and Analysis of an Ultra-Low On-Resistance Power Switch 4
Sylvester Ankamah-Kusi, Blake Travis, Swathi Kamath, Rajen Murugan, Tom Kronenberg

Signal Integrity of Die-To-Die Interface with Advanced Packages for Co-Packaged Optics 7
Jongchul Shin, Hamid Eslampour, Sangnam Jeong, Woopoung Kim, Seokbeom Yong, Sung-Oh Ahn, Eunkyeong Park, Sangsub Song

Delay Rational Macromodelling of Noisy Tabulated Frequency Responses 10
Alexander Kirchberger, Anestis Dounavis

Fan-Out Region Crosstalk Optimization of High-Density PCIe 6.0 SMT Connectors 13
Dan Liu, Yangfan Zhong, Minzheng Tian, Mengmeng Guo, Bing Wei, Weizhe Li, Jingbo Li, Tina Bao

Optimization of TSV Array Based on Mathematical Model for HBM3 16
Yen-Tung Chen, Yu-Ying Cheng, Tzong-Lin Wu

Application of the Reverse Pulse Technique for Worst Case Transient Analysis in HPC PDN Design 19
Chad M. Smutzer, Jordan R. Keuseman, Alexander P. Hickman, Clifton R. Haider

A DDR5 Interposer De-Embedding Method Based on Transfer Function 22
Aobo Li, Jun Wang, Yan Xu, Kangkang Zhang, Xiuqin Chu

A Hybrid Polynomial Chaos Expansion and Gaussian Process Regression Method for Forward Uncertainty Quantification of Integrated Circuits 25
Paolo Manfredi, Riccardo Trinchero

Parametric S-Parameter Prediction Using Deep Learning 28
Vinayak Bansal, Lihong Feng, Valentin De La Rubia, Peter Benner

Modeling Multiplexed Qubit Readout with a Josephson Traveling-Wave Parametric Amplifier 31
Samuel T. Elkin, Michael Haider, Thomas E. Roth

Comparative Evaluation of 100G-PAM4 Ethernet Link Performance in Air and Immersion Cooling Conditions 34
Dan Liu, Oluwafemi Akinwale, Yangfan Zhong, Kai Wang, Cesar Mendez-Ruiz, Kusuma Matta

Cascading of 2D and 3D Simulations of ASIC Substrate Interconnect Up to 100 GHz 37
Zhekun Peng, Junyong Park, Sathvika Bandi, Santosh Pappu, Srinivas Venkataraman, Xu Wang, Granthana Ranzaswamy, Donghyun Kim

Multiphysics Simulation and Measurement Correlation of a Multichip Module IC Package Current Sensor 40
Rajen Murugan, Jie Chen, Guangxu Li, Yutaka Suzuki, Sylvester Ankamah-Kusi

Impact of Non-Functional Pads Location on Eye Diagram Performance 43
Mehdi Mousavi, Kevin Cai, Junyong Park, Chaofeng Li, Manish K. Mathew, Reza Asadi, Shameem Ahmed, Donghyun Bill Kim, Bidyut Sen

High-Speed Interconnect Design of Silicon Interposer Based Heterogeneous Integration for AI Computing 46
Keeyoung Son, Seonguk Choi, Keunwoo Kim, Jiwon Yoon, Junghyun Lee, Haeseok Suh, Hyunjun An, Joungho Kim

Design and Analysis of L3 Cache Embedded-GPU-High Bandwidth Memory Architecture with Reduced Energy and Latency for AI Computing 49
Haeseok Suh, Jiwon Yoon, Keeyoung Son, Seonguk Choi, Keunwoo Kim, Junghyun Lee, Taein Shin, Hyunjun An, Taesoo Kim, Jungmin Ahn, Hyunah Park, Hyunsik Kim, Taeil Bae, Haekang Jung, Joungho Kim

Analysis of Nonlinear Phase Interactions of a Differential Line in the Presence of a Signal Skew 52
Byung Cheol Min, Mun Ju Kim, Hyun Chul Choi, Kang Wook Kim

A 155 MHz Low-Jitter PLL for Enhanced Signal Integrity in High-Speed Interconnects 55
Tiruye Mulat Ayinet, Gerba Olani Baissa, Teo T. Hui

Single-Layer Wiring Design in UCIe to Realize Low-Cost Interposer Substrate 58
Soshi Shimomura, Yutaka Uematsu, Katsuya Kikuchi, Haruo Shimamoto, Yuuki Araga, Shinichi Ouchi

PCIe Gen 6.0 SSD Receiver PAM-4 SI Analysis Based on End-Port Time-Domain Measurements for Unknown System Channel 61
Jinwook Song, Jinan Lee, Jonghee Jeong, Seokwoo Hong, Sungwoo Jin, Hyunwoo Kim, Sungwon Roh, Chorom Jang, Youngjun Ko, Taehyun Shim, Juneyoung Kim, Dongho Choi, Kyungsuk Kim, Sunghoon Chun

Using Generative AI to Predict DC Electrical Performance 64
J. Eric Bracken

PCIe Gen 6.0 SSD PSIJ Estimation Based on Early Design Stage Jitter Sensitivity Measurements 67
Youngjun Ko, Jinwook Song, Seokwoo Hong, Jinan Lee, Jonghee Jeong, Sungwoo Jin, Hyunwoo Kim, Chorom Jang, Sungwon Roh, Dongho Choi, Kyungsuk Kim, Sunghoon Chun

Application of CAMM2 Connector on PCIe Gen 6.0 SSD Host Interface for Low Near-End Crosstalk 70
Sungwoo Jin, Jinwook Song, Seokwoo Hong, Youngjun Ko, Hyunwoo Kim, Sungwon Roh, Chorom Jang, Dongho Choi, Kyungsuk Kim, Sunghoon Chun

An Efficient SPICE-Compatible Model for Fast Co-Simulation of Signal and Power Integrity on Multilayer PCB with Arbitrary Shape 73
Hyunwoo Kim, Dongryul Park, Seunghun Ryu, Seonghi Lee, Sanguk Lee, Jinwook Lee, Dongkyun Kim, Seungyoung Ahn

Latency Insertion Method for Fast Electro-Thermal Simulation of FinFET with Self-Heating Effect 76
Yi Zhou, José E. Schutt-Ainé

Eye-Diagram Edge Estimation (EEE) Network for Through Silicon Via Design in Next-Generation High Bandwidth Memory 79
Hyunjun An, Junghyun Lee, Keeyoung Son, Seonguk Choi, Taein Shin, Keunwoo Kim, Jiwon Yoon, Taesoo Kim, Jungmin Ahn, Hyunah Park, Haeseok Suh, Joungho Kim

Automated Accurate Quadratic Formulation of Nonlinear Circuits 82
Germin Ghaly, Emad Gad, Michel Nakhla

Crosstalk Analysis in Add-In Card Structure for High-Speed SerDes Channels with PCIe Gen6 85
Sungjin Yoon, Manho Lee, Kwangho Kim, Hyeongi Lee, Chulhee Cho, Youngjae Lee, Wooshin Choi, Young-Chul Cho, Jung-Hwan Choi, Young-Soo Sohn

Agile Analysis for Worst-Case Eye-Diagrams in Multi-Line Links of CoWoS Packaging 88
Zhu-Chen Chang, Chien-Min Lin, Ruey-Beei Wu

Operator Inference for Rigid-Flex Printed Circuit Boards Subject to Large Deformations 91
Pascal Den Boef, Diana Manvelyan, Wil Schilders, Joseph Maubach, Nathan Van De Wouw

A Signal Integrity Comparison of VIPPO Technology for PCIe 5.0 DC Blocking Capacitors 94
Andrew Page, Matteo Cocchini

Analysis of Interconnects in Multilayer SIW Bandpass Filters Design 97
Lu Qiu, Xiao-Wei Zhu, Xian-Long Yang

Yield-Aware Interposer Design for UCIe Interconnects 100
Ram Krishna, Ashita Victor, Srujan Penta, Xu Chen, Muhannad S. Bakir, Nam Sung Kim, Elyse Rosenbaum

Efficient Thermal Analysis for Heat Dissipation in Three-Dimensional Chip-Stacking Packaging 103
Cheng-Yuan Lu, Chien-Min Lin, Ruey-Beei Wu

Design of an Ultra-High-Speed Digital Interface Based on a Coplanar Stripline 106
Mun-Ju Kim, Byung-Cheol Min, Hyun-Chul Choi, Kang-Wook Kim

Design and Analysis of High-Density Silicon Interposer Channel and Power Distribution Network 109
Haeyeon Kim, Joonsang Park, Hyunah Park, Keeyoung Son, Hyunsik Kim, Taeil Bae, Haekang Jung, Joungho Kim

Signal Integrity Analysis of PCIe Channel with Floating Board-To-Board Connectors in Automotive Infotainment System 112
Junghyun Lee, Keeyoung Son, Junho Park, Joonsang Park, Keunwoo Kim, Hyunjun An, Seonguk Choi, Jihun Kim, Hyunah Park, Sumi Choi, Sanghyuk Son, Joungho Kim

Design and Analysis of Extended Scale Cache (ESC) Stacked-GPU-HBM Module Architecture Considering Power Integrity (PI) 115
Hyunah Park, Seonguk Choi, Haeyeon Kim, Taein Shin, Keeyoung Son, Jiwon Yoon, Junghyun Lee, Haeseok Suh, Taesoo Kim, Jungmin Ahn, Hyunjun An, Joungho Kim

Explainable Reinforcement Learning(XRL)-Based Decap Placement Optimization for High Bandwidth Memory (HBM) 118
Keunwoo Kim, Hyunwook Park, Keeyoung Son, Seonguk Choi, Taein Shin, Junghyun Lee, Jiwon Yoon, Hyunjun An, Haeyeon Kim, Wooshin Choi, Jung-Hwan Choi, Joungho Kim

Nonlinear Macromodeling of Voltage-Regulated Power Delivery Networks 121
Antonio Carlucci, Stefano Grivet-Talocia

Efficient Parametric Assessment of Worst-Case Voltage Droop in Power Delivery Networks 124
Tommaso Bradde, Antonio Carlucci, Riccardo Trinchero, Paolo Mandredi, Stefano Grivet-Talocia

Limit of the Impact of the Via Stub Length on the Via Impedance in Printed Circuit Boards 127
Katharina Scharff, Xiaomin Duan, Dierk Kaller

Reinforcement Learning Based Automatic Router for Power Delivery Network Prototypes 130
Felix Yuan, Abinash Roy

Improve CLK Phase Noise Performance by Mitigating Antiresonance Phenomenon of Power Net with a π-Type Filtering Structure... 133
Xinlin Tang, Shuxiang Li, Tao Fang, Yuan Fang

A Tunable Inductor Peaking Technique for Optical Communication Systems.. 136
Festim Iseini, Han-Ting Lin, Nicola Pelagalli, Andrea Malignaggi, Corrado Carta, Gerhard Kahmen, Andreas Weisshaar

Tunable True-Time-Delay Unit Based on Bridged T-Coil.. 139
Han-Ting Lin, Festim Iseini, Andreas Weisshaar

An Efficient Machine Learning Approach for PSIJ Analysis in a Chain of CMOS Inverters 142
Ahsan Javaid, Ramachandra Achar, Jai Narayan Tripathi

Modeling Microwave S-Parameters Using Frequency-Scaled Rational Gaussian Process Kernels................ 145
Thijs Ullrick, Dirk Deschrijver, Wim Bogaerts, Tom Dhaene

PSIJ Based Optimal PDN Design for Cost-Effective SSD Using Reinforcement Learning 148
Taein Shin, Seonguk Choi, Jungmin Ahn, Junghyun Lee, Keunwoo Kim, Haeseok Suh, Hyunah Park, Haeyeon Kim, Hyunjun An, Jinwook Song, Joungho Kim

A Study on How Capacitance of Power Filtering Circuit Influences the Antiresonance Frequency 151
Shuxiang Li, Xinlin Tang, Tao Fang, Yuan Fang, Greg Fu, Stephen Scearce

Simulation Method for Quasi-Static Solver to Effectively Model Parasitic Components Between Package and PCB 154
Silvia Simone, Fabio Pareschi, Davide Lena, Gianluca Setti

Analysis of Echo and Crosstalk Cancellation in Simultaneous Bidirectional Transceivers for Dense Die-To-Die Interconnects 157
Tong Liu, Taeyang Sim, Samuel Palermo

Transformer Based Channel Identification... 160
Priyank Kashyap, Yeujiang Wen, Yongjin Choi, Chris Cheng, Paul D. Franzon

Design and Analysis of Ultra High Bandwidth (UHB) Interconnection-Based GPU-Ring for the AI Superchip Module 163
Jungmin Ahn, Seonguk Choi, Taein Shin, Junghyun Lee, Jiwon Yoon, Keunwoo Kim, Keeyoung Son, Haeseok Suh, Taesoo Kim, Hyunah Park, Hyunjun An, Jinwook Song, Joungho Kim

Recent Advances in Signal Integrity Simulation and Analysis of Interposers.. 166
Jonatan Aronsson, Feng Ling

Multiphysics-Informed ML-Assisted Chiplet Floorplanning for Heterogeneous Integration 169
Vinicius C. Do Nascimento, Seunghyun Hwang, Michael J. Smith, Qiang Qiu, Cheng-Kok Koh, Ganesh Subbarayan, Dan Jiao

Accuracy Study of the Differential Surface Admittance Operator for Lossy Metal Characterization.............. 172
M. Huynen, V. Okhmatovksi, D. De Zutter, D. Vande Ginste

Compact Fiber Weave Model for Full Wave Solvers 175
Stefan De Araujo, Daniel De Araujo, Bhyrav Mutnury

Megtron 6 and 8 Characterization Methodology 178
Stefan De Araujo, Daniel De Araujo, Roger Delbue, Ryan Keegan

Full-Wave Analysis for Ground Via Placement with Layered Media Integral Equations 181
Alireza Niazi, Vladimir Okhmatovski

Tree-Based Boosting for Efficient Estimation of S-Parameters for Package Electrical Analysis 184
Doganay Özese, Mustafa Gökçe Baydogan, Ahmet Cemal Durgun, Kemal Aygün

Causal RL Prediction of Fine-Pitch Interconnects Using Neural Networks 187
Hasan Said Ünal, Ahmet Cemal Durgun

A Robust Optimization Approach for High Bandwidth Memory Interposer Using Machine Learning 190
Anandajith Jinesh, Xuan Chen

Hand-Drawn Circuit Schematic Digitization and Netlisting Using Machine Learning with Emphasis on Signal Integrity Applications 193
Anuj Mathur, Ramachandra Achar

Analysis and Modeling of Controlled Silicon Substrate Roughness for Silver-Based Backside Metallization in Power Electronics Packaging 196
Mohamed Lamine Faycal Bellaredj, Goran Miskovic, Lukas Vojkuvka

Worst-Case Voltage Droop Using Peak Distortion Analysis 199
Mohamed Sahouli, Isaac Ali, David Reinamendivil, Gerry Talbot

Equalization Techniques for Time Domain Signaling 202
Shakib Mahmood, Parneet Tethy, Richelle L. Smith, Carl W. Werner, Masum Hossain

A Highly-Scalable Parallel Boundary Element Method for the Full-Wave Electromagnetic Analysis of Large Interconnect Networks and Entire Packages 205
Damian Marek, Jasper Hatton, Yongzhong Li, Piero Triverio

Gradient-Based Method to Find Solution for Rational Polynomial Chaos Coefficients for Uncertainty Quantification 208
Karanvir S. Sidhu, Roni Khazaka

On the Parallelization of the MultiAIM Algorithm for the Fast Electromagnetic Analysis of 3D ICs 211
Yongzhong Li, Piero Triverio

Author Index