

2024 IEEE Silicon Nanoelectronics Workshop (SNW 2024)

**Honolulu, Hawaii, USA
15-16 June 2024**



IEEE Catalog Number: CFP24SNW-POD
ISBN: 979-8-3503-9164-0

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***** *This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24SNW-POD
ISBN (Print-On-Demand):	979-8-3503-9164-0
ISBN (Online):	979-8-3503-9163-3
ISSN:	2161-4636

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

Table of Contents

Opening Remarks

Peide Ye & Zihong Chen, Purdue University

Session 1: Plenary

Session Chair: *Pei-Wen Li, NYCU*

1.1 (Keynote) Future Perspectives of CMOS Logic Innovation Beyond 2nm, T. Hiramoto¹, H. Wakabayashi², ¹University of Tokyo, ²Tokyo Inst. of Tech.	1
1.2 (Keynote) Gate Oxide Reliability: Upcoming Trends, Challenges and Opportunities, B. Kaczer¹, R. Degraeve¹, J. Franco¹, T. Grasser², Ph. J. Roussel¹, E. Bury¹, P. Weckx¹, A. Chasin¹, S. Tyaginov¹, ¹imec, ²TU Vienna	3

Session 2: GAA/Nanosheet Transistors I

Session Chair: *Takahiro Shinada, Tohoku University*

2.1 (Invited) Heterogeneous CFET: A Pathway to CMOS Performance Balance Engineering, X.-R. Yu¹, W.-H. Lu¹, S.-W. Chang¹, W.-H. Chang², Darsen D. Lu¹, Y.-J. Lee^{3,4}, T. Maeda³, W.-F. Wu⁴, Y.-M. Li³, Y.-H. Wang¹, ¹Natl. Cheng Kung University, ²AIST, ³National Yang Ming Chiao Tung University, ⁴TSRI	5
2.2 Enhanced Electrical Performance of Ultrathin Body Nanosheets, B.-W. Huang, Y.-R. Chen, T. Chou, H.-C. Lin, C.-T. Tu, Y.-C. Liu, W.-H. Hsieh, W.-J. Chen, M.-K. Lin, Y.-Q. Liu, L.-K. Wang, H.-C. Chou, Y. Huang, D.-W. Lin, C.-W. Liu, National Taiwan University	7

Session 3: Quantum Computing Devices/Circuits

Session Chair: *Louis Hulin, CEA-Leti*

3.1 (Invited) Integration Technology for Superconducting Quantum Circuits, Shiro Kawabata, AIST	9
3.2 Demonstration of 99.9% Single Qubit Control Fidelity of a Silicon Quantum Dot Spin Qubit Made in a 300 mm Foundry Process, N. D. Stuyck^{1,2}, F. Mengke^{1,2}, W. H. Lim^{1,2}, S. S. Ramirez^{1,2}, C. Escott^{1,2}, T. Botzem^{1,2}, T. Tanttu^{1,2}, H. Yang^{1,2}, A. Saraiva^{1,2}, A. Laucht^{1,2}, S. Kubicek³, J. Jussot³, S. Beyne³, B. Raes³, C. Godfrin³, D. Wan, K. D. Greve^{3,4}, A. Dzurak⁴, ¹Diraq, ²UNSW, ³imec, ⁴KU-Leven	11

3.3 Tunneling Current Spectroscopy of Self-assembled Ge Double Quantum Dots with Hard-wall Barrier Engineering, Y.-W. Chiu, I. H. Wang, T. Tsai, H.-C. Lin, P.-W. Li, National Yang Ming Chiao Tung University	N/A
---	-----

Session 4: Memory Technology

Session Chair: *Jiezhi Chen, Shandong University*

4.1 (Invited) IGZO Channel VCT (Vertical Channel Transistor) Technology for sub-10nm DRAM : Challenges and Opportunities, Y. Lee, Daewon Ha, W. Lee, S. Yoo, J. H. Bae, M. H. Cho, K. Yoo, S. M. Lee, S. Lee, M. Terai, T. H. Lee, K. J. Moon, C. Sung, M. Hong, D. G. Cho, H. Kim, J. H. Seo, K. Park, B. J. Kuh, S. Hyun, S. J. Ahn, and J. H. Song, Samsung Electronics	15
4.2 A Novel 2-Tier Stacked Vertical Channel GAA Transistor Architecture with Area-Saving 3-Dimensional Local Interconnect to Achieve Gb-Density 6T SRAM with Acceptable Low Standby Chip Leakage (~1mA), H.-T. Lue, W. Chen, T.-H. Yeh, K.-C. Wang, and C.-Y. Lu, Macronix	17
4.3 A Comparative Study of HBL and VBL 3D DRAM: Signal Margin, Bit-cell Density, and Scalability, X. Wu¹, L. Upton¹, P.-K. Hsu², J. Chen¹, S. Yu², H.-S. P. Wong¹, ¹Stanford University, ²Georgia Institute of Technology	19
4.4 Impact of Proton Irradiation on SiNx and Si–SiO₂ Interfaces in FLASH Memory, H. Kim¹, J. Park¹, J. Im², H. Kim², Y. Jun Yoon³, Y.-M. Kim⁴, K. Park⁵, S. Y. Woo², J.-H. Bae¹, ¹Kookmin University, ²Kyungpook National University, ³Andong National University, ⁴Korea Atomic Energy Research Institute, ⁵Yonsei University	N/A
4.5 A Novel RRAM-based Ternary Strong-PUF with High Security Intensity Feasible for Low-earth Orbit Satellites in the 6G Era, S. H. Lin, E. R. Hsieh, National Central University	23

Session 5: Ferroelectric Memory

Session Chair: *K. Toprasertpong, The Univ. of Tokyo*

5.1 (Invited) Outlook and Prospects for Ferroelectric Augmentation of Vertical NAND Flash Technology, Asif Khan, Georgia Institute of Technology	N/A
---	-----

5.2 Investigating the Correlation Between Material Ferroelectricity and Silicon-Channel FeFET Performances: Insights for Material Engineering in Device Optimization, X. Wang, L. Jiao, Z. Zhou, Z. Zheng, Y. Chen, R. Shao, C. Sun, D. Zhang, G. Liu, X. Gong, National University of Singapore	N/A
5.3 Ferroelectricity Engineered AlScN Thin Films Prepared by Hydrogen Included Reactive Sputtering for Analog Applications, S.-M. Chen¹, H. Nishida¹, T. Hoshii¹, K. Tsutsui¹, H. Wakabayashi¹, Edward Y. Chang², and K. Kakushima¹ Tokyo Inst. of Technology, National Yang Ming Chiao Tung Univ.	29
5.4 Investigation of HfO₂ and ZrO₂ Nanolamination Thickness on Superlattice HZO FeRAMs Exhibiting Enhanced Remnant Polarization and Improved Endurance, D. R. Hsieh, Z. Y. Hong, W. J. Yeh, J. C. Ni, H. E. Luo, Y.-K. Liang, S. L. Hsieh, K. L. Chen, T.-S. Chao, National Yang Ming Chiao Tung University	31
5.5 Impact of Time Delay Schemes on Reliability Degradation During Program/Erase Cycling in HZO-based FeFETs, X. Li¹, G. Zhao¹, L. Tai¹, P. P. Sang¹, X. Dou¹, X. Zhan¹, X. Wang², J. Wu¹, J. Chen¹, ¹Shandong University, ²Institute of Microelectronics of Chinese Academy of Sciences	33
5.6 Study on the Anomalous Characteristics of Random Telegraph Noise in FeFETs, P. Cai¹, Y. Wu², Z. Sun¹, H. Li¹, X. Wang³, Z. Ji², R. Wang¹, R. Huang¹, ¹Peking University, ²Shanghai Jiao Tong University, ³Institute of Microelectronics of Chinese Academy of Sciences	35
Session 6: Neuromorphic Computing	
<i>Session Chair: Takahide Oya, Yokohama National University</i>	
6.1 Reservoir Computing Using Nonlinear Polarization and Charge Dynamics of Anti-ferroelectric HZO/Si FETs, S.-Y. Min, K. Toprasertpong, E. Nako, R. Nakane, M. Takenaka, S. Takagi, The University of Tokyo	37
6.2 Design Space Trade-offs in Networks of Coupled Injection-locked Ring Oscillators for Ising-based Optimum Search, A. Bazzi, F. Badets, L. Hutin, CEA-Leti	39
6.3 Background-Pattern-Dependency-Tolerant Weight Transfer Method for Accurate NAND-Flash Based Spiking Neural Networks,	41

B. Jeon, J. H. Chang, W. Y. Choi, Seoul National University

6.4 Artificial VO₂ Spiking Neurons with Protective Mechanism for Enhancing Resilience of Spiking Neural Network Against Adversarial Attacks, C. Ban¹, L. Shan¹, G. Yang¹, J. Gao¹, L. Wu¹, Z. Wang^{1,2}, Y. Cai^{1,2}, R. Huang^{1,2}, ¹Peking University, ²Beijing Advanced Innovation Center for Integrated Circuits	43
6.5 Flash-based Computing-in-Memory (CiM) Towards Stochastic Computing with Low Power-consumption and High Noise-immunity, H. Wang, Y. Feng, X. Zhan, M. Bai, P. P. Sang, J. Wu, Q. Wang, J. Chen, Shandong University	45

Session 7: GAA/Nanosheet Transistors II

Session Chair: Woo Young Choi, SNU

7.1 (Invited) Multi-Vt Gate Stack Technologies for Nanosheet and CFET Devices, H. Arimura¹, J. Franco¹, L.-Å. Ragnarsson¹, A. Vandooren¹, S. Brus¹, W. Maqsood¹, T. Conard¹, G. Alessio Verni², J. W. Maes², B. Kannan², M. Givens², N. Horiguchi¹, ¹imec, ²ASM	47
7.2 Investigation of Sheet Width Dependence on Hot Carrier Degradation in GAA Nanosheet Transistors, Z. Sun, Z. Wang, R. Wang, R. Huang, Peking University	49

Session 8: Process and Transistor Technology

Session Chair: Xiao Gong, NUS

8.1 Investigating HfO₂/ZrO₂ Superlattice Dielectric with High-κ Value of 52 via Annealing Temperature and Layer Thickness Modulation Beyond Moore's law, Y. C. Wu¹, Y.-J. Yao¹, H. J. Chang¹, C.-Y. Wei¹, Y.-M. Fu¹, B.-X. Chen¹, T.-J. Lin¹, Y.-T. Fang¹, G.-L. Luo² and F.-J. Hou², ¹National Tsing Hua University, ²Taiwan Semiconductor Research Institute	N/A
8.2 First Demonstration of SRAM Transistor Based on 3-dimensional Stacked FET with Back Side Interconnection Structure Beyond 1nm Node, M. Kim^{1,2}, J. Park², S. Park², J. Park², J. Kim¹, D. Ha², H. Shin^{1,3}, ¹Seoul National University, ²Samsung, ³Integra Semiconductor	53
8.3 High Performance Te/ZnO CMOS Inverter Operated at 77K, M. Kim, K. Kim, K. Kim, J. H. Jun, H.-W. Lee, B. H. Lee, Pohang University of Science and Technology	N/A

8.4 Steep Slope Device N-type Gate-Controlled Carrier-Injection SOI-Transistor: Suppression of Hysteresis by Ar-ion Implantation and Possibility of CMOS, H. Yonezaki, T. Mori, J. Ida, Kanazawa Institute of Technology	57
---	-----------

Session 9: 2D Materials and Oxide Semiconductor Devices for 3D integration

Session Chair: Byoung Hun Lee, POSTECH

9.1 (Invited) Potential and Challenges of 2D Materials Based Electronics, L.-J. Li, University of Hong Kong	N/A
--	------------

9.2 A Nanosheet Oxide Semiconductor FET Using ALD InZnOx Channel, S.-H. Kim, K. Hikake, Z. Li, T. Saraya, T. Hiramoto, M. Kobayashi, University of Tokyo	61
---	-----------

9.3 Investigation of In-Sn-Zn Composition on the Characterization of Submicron Channel Length Ultra-Thin Atomic Layer Deposited InSnZnO Channel Transistors, Y.-K. Liang^{1,2}, L.-C. Peng¹, Y.-L. Lin¹, J.-Y. Zheng¹, D. R. Hsieh¹, T.-T. Chou³, H.-Y. Huang⁴, Y.-M. Lin⁴, Y.-C. Tseng¹, T.-S. Chao¹, E. Y. Chang¹, K. Toprasertpong², S. Takagi², C.-H. Lin¹, ¹National Yang Ming Chiao Tung University, ²The Univ of Tokyo, ³Taiwan Instrument Research Institute, ⁴Taiwan Semiconductor Manufacturing Company	63
---	-----------

9.4 BEOL-Compatible In₂O₃ Thin-Film Transistor with Linear Dielectric ZrO₂ Achieving Dielectric Constant over 27 and Enhanced Field-Effect Mobility up to 89.3 cm²/V·s, Z. Lin, P. Ye, Purdue University	65
---	-----------

9.5 First Investigation of Low-Frequency Noise in Scaled Atomic-Layer-Deposited IGZO FETs with Different Indium Ratio, S. Lee, C. Niu, Z. Zhang, Y. Zhang, L. Long, Z. Lin, H. Wang, P. Ye, Purdue University	N/A
--	------------

9.6 A Novel Ternary Transistor with Nested Source Design Incorporating Hybrid Switching Mechanism for Low-Power and High-Performance Applications, S. Xu¹, L. Tianyang¹, T. Luo¹, R. Huang^{1,2}, Q. Huang^{1,2}, ¹Peking University, ²Beijing Advanced Innovation Center for Integrated Circuits	69
---	-----------

Session 10: Poster Session 1

Session Chairs: Steve Chung, National Yang Ming Chiao Tung University

P1-1 Single Electron Charge Detection in Nanoscale Metal Double-dot: DC Single Electron Transistor vs. gate RF sensing, M. I. Rahaman¹, G. Szakmany¹, X. Jehl², A. Orlov¹, G. Snider¹, ¹University of Notre Dame, ²Univ. Grenoble Alpes	71
P1-2 Ferromagnetic Manganese Silicide Nanoparticles Formed by Ion Implantation in Silicon, R. Ohsugi, M. Kawano, Y. K. Wakabayashi, Y. Krockenberger, H. Sumikura, J. Noborisaka, K. Nishiguchi , NTT	73
P1-3 The Simulation of Double Germanium Quantum Dots in a Ring-Shaped Quantum Structure, C. Liang, Y.-T. E. Tang, National Central University	75
P1-4 Improved Uniformity and Excellent Endurance Characteristics of TaOx-Based RRAM by Laser-Mediated Interface Engineering, L. Wu¹, Q. Wang¹, H. Liao¹, C. Ban¹, L. Shan¹, Z. Wang^{1,2}, Y. Wang^{1,2}, Y. Cai^{1,2}, ¹Peking University, ²Beijing Advanced Innovation Center for Integrated Circuits	77
P1-5 Effects of Modulation Pulse on Resistive Switching Dynamics of RRAM Devices, C.-H. Chien, Y.-H. Wang, National Cheng Kung University	79
P1-6 Innovative Switching Mechanism, Performance Investigations and Scaling Effects in a-V₂O₃ Based ReRAM devices, K. Veyret^{1,2}, L. Laborie¹, R. Bon¹, G. Navaro¹, R. Hida¹, N. Castellani¹, C. Carabasse¹, P. Gonon¹ and E. Jalaguier¹, ¹CEA-Leti, ²Univ. Grenoble Alpes	81
P1-7 Floating Gate Field Effect Transistors for Logic-In-Memory Application, S. Jae Baik¹, S. Kim², M. Kang³, and J. Jeon², ¹Samsung Electronics, ²Sungkyunkwan University, ³Korea National University of Transportation	N/A
P1-8 Withdrawn	
P1-9 High Performance HfLaO-based TiO₂-Channel FE V-NAND with High Consistency and Low Operation Voltage, X. Song, S. Li, D. Sun, X. Liu, J. Kang, Peking University	85
P1-10 Accelerated Program Inhibition Failure by Trap-Mediated Tunneling in the Polycrystalline Floating-Channel 3-D NAND Flash Memory Array, S. Kim¹, U. Lee², Y. Lee¹, C. Ahn², J. Sim², S. Cho¹, ¹Ewha Womans University, ²SK hynix inc.	87
P1-11 Investigation of Row Hammer and Passing Gate Effects Based on the Work Functions of Dual Gates in DRAM Cells, H. Kim¹, J. Im¹, J. Kim¹, S. Woo¹, T. Kwon¹, Y. J. Yoon², J.-H. Bae³, S. Y. Woo¹, ¹Kyungpook National University, ²Andong National University, ³Kookmin University	89
P1-12 Analysis of Row Hammer and Passing Gate Effect in DRAM Cells by BCAT	91

Structural Design, J. Im¹, H. Kim¹, J. Kim¹, S. Woo¹, T. Kwon¹, Y. J. Yoon², J.-H. Bae³, S. Y. Woo¹, ¹Kyungpook National University, ²Andong National University, ³Kookmin University

P1-13 Controllable Polarization Switching of Hafnia-Based Ferroelectric Bilayers, J. Jeong, H. Park, J. Woo, Kyungpook National University 93

P1-14 Short-term and Long-term T-O Phase Transition Responsible for Two stages of Wake-up Process in Ferroelectric Hf_{0.5}Zr_{0.5}O₂ Film, D. Chen, G. Qiang, F. Yuyan, Y. Zikang, J. Liu, S. Mengwei, L. Xiuyan, Shanghai Jiao Tong University 95

P1-15 Enhancing Annealing Strategies for Back-End-of-Line-Compatible HfO₂-Based Ferroelectric Capacitors with Time Periods and Gas Species, C.-H. Wu¹, T.-Y. Lin², C.-Y. Chiu², C.-J. Su², V. P.-H. Hu¹, ¹National Taiwan University, ²National Yang Ming Chiao Tung University N/A

P1-16 Plasma-enhanced Atomic Layer Deposition Based FEFETs, C. Park^{1,2}, P. V. Ravindran¹, D. Das³, P. G. Ravikumar¹, W. Chern¹, S. Yu¹, A. I. Khan¹, ¹Georgia Institute of Technology, ²SK hynix , ³NIT Silchar N/A

P1-17 Investigation on the Local Polarization Scheme in Ferroelectric Tunnel Field-Effect Transistors for Ternary Content-Addressable Memory Applications, M. Ryu, J. S. Woo, W. Y. Choi, Seoul National University 101

P1-18 Study of Spacing-induced Fringing Effects on Emerging CFET Technology Nodes, Y.-Z. Chen¹, N. Thoti², Y.-T. E. Tang¹, ¹National Central University, ²University of Oulu 103

Session 11: Poster Session 2

Session Chairs: *K. Kakushima, Tokyo Institute of Technology*

P2-1 Compact Model of Feedback Field-Effect Transistor Using Artificial Neural Network, J. S. Su, J. H. Oh, Y. S. Yu, Hankyong National University 105

P2-2 Neural Encoder Using “PN-Body Tied SOI-FET”, M. Kobayashi, J. Ida, T. Mori, Kanazawa Institute of Technology 107

P2-3 Engineering Strategies in HfOx RRAM-Based Analog Synapses Toward Linear Weight Update for Neuromorphic Hardware Accelerators, Y. Kim, H. Choi, J. Woo, Kyungpook National University 109

P2-4 Enhancing Single-Electron Reservoir Computing Performance with Delay Function and Multiple-layer Reservoir Circuits, S. Watanabe, T. Oya, Yokohama National University 111

P2-5 Design of Single-Electron Circuit Representing Brownian Motion of Particles to 113

Implement Circuit Capable of Computing Diffusion Limited Aggregation Model, R. Miyakoshi, T. Oya, Yokohama National University

P2-6 A Machine-Learning-based Model for Emerging Memories Featuring Multiple States, Z. Wang¹, Z. Rong², R. Wang³, M. Chan², L. Zhang¹, ¹Peking University Shenzhen, ²Hong Kong University of Science and Technology, ³Peking University 115

P2-7 Automated Recipe Creation and Verification of Single Wafer Wet Etching: Ensemble Learning with Backcasting and Forecasting AIs Using Scarce Data, K. Shibata¹, H. Horiguchi², C. Matsui¹, K. Takeuchi¹, ¹University of Tokyo, ²SCREEN Semiconductor Solutions Co., Ltd. 117

P2-8 Design of the 2-nm Nanosheet NAND-type TCAM with High Speed and Compat Cell-size: 45% Layout-reduction of 3-nm TCAM, L.-A. Yu, C.-Y. Chou, C.-C. Lin, T.-Y. Tsai and E. R. Hsieh, NCU 119

P2-9 Design of Single-electron Information-processing Circuit for Particle Computation, S. Mizuno, T. Oya, Yokohama National University 121

P2-10 Predicting the Retention Property of Scaled Cylindrical IGZO 2T0C DRAM Cells, S.-M. Jeong, S. -M. Hong, GIST 123

P2-11 Withdrawn N/A

P2-12 Withdrawn

P2-13 Simulation of Trap-Induced Noise Characteristics in 3-nm Complementary FET, J. Xu, Z. Zhou, F. Liu, X. Liu, Peking University 127

P2-14 Simultaneously Improved Electrical Characteristics of Ge n/p-FinFETs by Using HfN Interface Layer with In-Situ Plasma Oxidation Treatments, K.-S. Chang-Liao¹, Y.-Y. Chen², D.-B. Ruan¹, C.-H. Li¹, ¹National Tsing Hua University, ²Fuzhou University N/A

P2-15 High Performance Ge FinFET CMOS Invertor with Post Plasma Oxidation and Nitridation Treatments before Supercritical Fluid Process, K.-S. Chang-Liao¹, W.-C. Hung², D.-B. Ruan¹, K.-C. Yang¹, ¹National Tsing Hua University, ²Fuzhou University N/A

P2-16 Characteristics of Aluminum-based Oxide with ALD SiO₂ Interfacial Layer as the Gate Dielectric of the Silicon Carbide (SiC) MOS Capacitor with RTA Annealing, C.-L. Lin, B. X. Su, Y. L. Lee, Feng Chia University 133

P2-17 Electrical Characteristics of BEOL-Compatible Top-Gate In₂O₃ Transistors, P. Hong J. Hao, X. Li, Huazhong University of Science and Technology 135