2024 IEEE 35th International Conference on Application-specific Systems, **Architectures and Processors** (ASAP 2024)

Hong Kong 24-26 July 2024



IEEE Catalog Number: CFP24063-POD **ISBN:**

979-8-3503-4964-1

Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

FP24063-POD
9-8-3503-4964-1
9-8-3503-4963-4
60-0511
/

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400 Fax: (845) 758-2633 E-mail: curran@proceedings.com Web: www.proceedings.com



2024 IEEE 35th International Conference on Applicationspecific Systems, Architectures and Processors (ASAP) **ASAP 2024**

Table of Contents

Preface	xi
Message from the Chairs	xii
Organizing Committee	xiv
Program Committee	xvi
Reviewers	xviii
Sponsors	xx

2024 IEEE 35th International Conference on Application-Specific Systems, Architectures and Processors

Multi-Level Prototyping of a Vertical Vector AI Processing System
SpDCache: Region-Based Reduction Cache for Outer-Product Sparse Matrix Kernels
CoNAX: Towards Comprehensive Co-Design Neural Architecture Search Using HW Abstractions 8 Yannick Braatz (Robert Bosch GmbH, Germany), Taha Soliman (Robert Bosch GmbH, Germany), Shubham Rai (Robert Bosch GmbH, Germany), Dennis Sebastian Rieber (Robert Bosch GmbH, Germany), and Oliver Bringmann (Eberhard Karls Universität Tübingen, Germany)

An End-to-End Agile Design Framework to Improve Energy Efficiency on CGRAs
Fault-Tolerant DAG Scheduling with Runtime Reconfiguration on Multicore Real-Time Systems 19 Yuanhai Zhang (Sun Yat-sen University, China), Shuai Zhao (Sun Yat-sen University, China), Gang Chen (Sun Yat-sen University, China), and Kai Huang (Sun Yat-sen University, China)
Design Space Exploration of Semantic Segmentation CNN SalsaNext for Constrained Architectures
 Memory Access Acceleration Through Architecture Design for Edge SoCs
ZeroVex: A Scalable and High-Performance RISC-V Vector Processor Core for Embedded Systems 32 Tenghao Zhao (Tsinghua University, China) and Zhaohui Ye (Tsinghua University, China)
MSCA: A Multi-Grained Sparse Convolution Accelerator for DNN Training
BitShare: An Efficient Precision-Scalable Accelerator with Combining-Like-Terms GEMM
Configurable Loop Shuffling via Instruction Set Extensions
Deoxys: Defensive Approximate Computing for Secure Graph Neural Networks
A Framework for Generating Accelerators for Homomorphic Encryption Operations on FPGAs 61 Yang Yang (University of Southern California), Rajgopal Kannan (DEVCOM Army Research Office), and Viktor Prasanna (University of Southern California)
Real-Time Order Book Building and Snapshot Generating for High Frequency Trading on FPGA71 Yao Liu (China Securities Co., Ltd, China), Shiyang Chen (China Securities Co., Ltd, China), Long Ma (China Securities Co., Ltd, China), Guolong Yang (China Securities Co., Ltd, China), and Kun Wan (China Securities Co., Ltd, China)

A FPGA-HBM-Based Hardware Streaming Accelerator for GNN Sampling
A DRL-Based Multi-Priority Task Division Scheduling Strategy in IIoT
 TwinStep Network (TwNet): a Neuron-Centric Architecture Achieving Rapid Training
Analysis and Optimization of Block LU Decomposition for Execution on Tightly Coupled Processor Arrays
Accelerating MRI Uncertainty Estimation with Mask-Based Bayesian Neural Network
Out-of-Order and Recursive RAS: A Return Address Stack Design On High Performance Processor
 SPARKLE: A 1,024-Core/16,384-Thread Single FPGA Many-Core RISC-V Barrel Processor Overlay 118 Riadh Ben Abdelhamid (Heidelberg University, Germany), Vladislav Valek (Heidelberg University, Germany), and Dirk Koch (Heidelberg University, Germany)
Design Space Exploration of FFT Accelerators for IEEE 802.11ax Using High-Level Synthesis 120 Uyong Lee (Konkuk University, South Korea), Yeji Park (LG Electronics, South Korea), Junsu Heo (Konkuk University, South Korea), Sungkyung Park (Pusan National University, South Korea), and Chester Sungchung Park (Konkuk University, South Korea)

 Sparm: A Sparse Matrix Multiplication Accelerator Supporting Multiple Dataflows
 Extending the RISC-V Instruction Set for High Performance Data Compression Hardware Acceleration
 MDCRA: A Reconfigurable Accelerator Framework for Multiple Dataflow Lanes
RO-SVD: A Reconfigurable Hardware Copyright Protection Framework for AIGC Applications 135 Zhuoheng Ran (City University of Hong Kong, China), Abdelgawad Muhammad A.A. (City University of Hong Kong, China), Zekai Zhang (City University of Hong Kong, China), Ray C.C. Cheung (City University of Hong Kong, China), and Hong Yan (City University of Hong Kong, China)
 Analyzing GPU Energy Consumption in Data Movement and Storage
 k-way In-Place Merge by CPU-GPU Cooperative Processing
CSIFA: A Configurable SRAM-Based In-Memory FFT Accelerator
A Convolutional Spiking Neural Network Accelerator with the Sparsity-Aware Memory and Compressed Weights

Spatzformer: An Efficient Reconfigurable Dual-Core RISC-V V Cluster for Mixed Scalar-Vector Workloads
Matteo Perotti (ETH Zurich, Switzerland), Michele Raeber (ETH Zurich, Switzerland), Mattia Sinigaglia (Università di Bologna, Italy), Matheus Cavalcante (ETH Zurich, Switzerland), Davide Rossi (Università di Bologna, Italy), and Luca Benini (ETH Zurich, Switzerland; Università di Bologna, Italy)
 SLICE Matrix: A Memory Access Scheduling Policy for Multicore Network Processors
 Enhancing a Hearing Aid Processor with ISA Extensions Supporting Flexible Fixed-Point Formats
MLIR-to-CGRA: A Versatile MLIR-Based Compiler Framework for CGRAs
Design of Light-Weight Encryption Algorithm Based on RISC-V Platform
 Raising Compute Density of Molecular Dynamics Simulation Through Approximate Memoization 195 Salim Khemira (University of Toronto, Canada), Xinyuan Wang (University of Toronto, Canada), Anh Nguyen (Fujitsu Laboratories, Japan), Yutaka Tamiya (Fujitsu Laboratories, Japan), Makoto Taiji (RIKEN Center for Biosystems Dynamics Research, Japan), Takahide Yoshikawa (Fujitsu Laboratories, Japan), and Jason Anderson (University of Toronto, Canada)
Leveraging MLIR for Efficient Irregular-Shaped CGRA Overlay Design
xTern: Energy-Efficient Ternary Neural Network Inference on RISC-V-Based Edge Systems
LLM Based End-to-end Branch Predictor Optimization Generator
Multiplier Design Addressing Area-Delay Trade-offs by Using DSP and Logic Resources on FPGAs

A Full-System Approach to Multi-Valued Logic Design
CHIME: Energy-Efficient STT-RAM-Based Concurrent Hierarchical In-Memory Processing
ISP2DLA: Automated Deep Learning Accelerator Design for On-Sensor Image Signal Processing 237 Dong-eon Won (Hanyang University, South Korea), Yeeun Kim (Hanyang University, South Korea), Janghwan Lee (Hanyang University, South Korea), Minjae Lee (Hanyang University, South Korea), Jonghyun Bae (SK hynix Inc., South Korea), Jongjoo Park (SK hynix Inc., South Korea), Jeongyong Song (SK hynix Inc., South Korea), and Jungwook Choi (Hanyang University, South Korea)
Voltage Range Evaluation of an Optically Reconfigurable Gate Array VLSI
Lightweight Extension of RISC-V Core for NTT-Like Algorithms
A LLC-Friendly LSM-Tree
Research on High-Efficiency Asynchronous Superscalar Processors
 Design of High-Performance while Energy-Efficient Microprocessor with Novel Asynchronous Techniques (PhD Forum Paper)

uthor Index	249