

2024 2nd International Symposium of Electronics Design Automation (ISEDA 2024)

**Xi'an, China
10-13 May 2024**



**IEEE Catalog Number: CFP24NZ9-POD
ISBN: 979-8-3503-5204-7**

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP24NZ9-POD
ISBN (Print-On-Demand):	979-8-3503-5204-7
ISBN (Online):	979-8-3503-5203-0

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2024 International Symposium of Electronics Design Automation (ISED A 2024)

Table of Contents

Preface.....	xv
ISED A 2024 Committee	xvi

❖ Chapter 1: Technology & Model

Knowledge-Guided Neural Network Based Nonlinear Current Model with Combined Loss Function	1
<i>Junjun Qi, Hongliang Lu, Silu Yan, Zhiwu Jiang, Lin Cheng, Yuming Zhang</i>	
Migrating Standard Cells for Multiple Drive Strengths by Routing Imitation	5
<i>Xiaohan Gao, Haoyi Zhang, Zhu Pan, Yibo Lin, Runsheng Wang, Ru Huang</i>	
Automatic Design of Structural Parameters for GaN HEMT Using Genetic Algorithm and Artificial Neural Networks	11
<i>Wei Du, Jing Chen, Jiahao Wu, Qing Yao, Yufeng Guo</i>	
A Verilog-A Compact Model for Four-Wave Mixing Supporting Electronic-Photonic Co-Simulation	16
<i>Siyuan Zhang, Xiaolong Fan, Nuo Chen, Ken Xingze Wang, Jing Xu, Min Tan</i>	
Physical Insight into Single-Event Upsets of DICE Circuits and Hardening Strategy	20
<i>Yutao Chen, Linlin Cai, Jianwen Lin, Zhengxin Zhang, Wangyong Chen, Yi Sun, Haiming Zhang</i>	
Recent Progress of AlGaIn/GaN HEMTs QPZD Model	26
<i>Xiang Su, Shuman Mao, Yuehang Xu</i>	
Modeling and Circuit Implementation of Complex Nonlinear Component Behavior Based on Attention-Assisted BiLSTM.....	32
<i>Zeng Hui Chang, Hong Cai Chen</i>	
Modeling the Temperature-dependence of Silicon Diode with Fermi-Dirac Statistics down to 50K.....	37
<i>Xinyue Zhang, Fangxing Zhang, Cong Shen, Zirui Wang, Runsheng Wang, Lining Zhang, Ru Huang</i>	
Atomic Level to Device Level Simulation of Transistor's Reliability	42
<i>Yue-Yang Liu</i>	
Heat Generation Counted by Phonon Absorption and Emission in GAA FET under the Framework of Non-Equilibrium Green's Function Method.....	44
<i>Hongwei Zhou, Zifeng Wang, Suteng Zhao, Deming Zhang, Lang Zeng</i>	

Simulation Study of Gate-All-Around TFET Based on Polarization Effect	50
<i>Yunhe Guan, Zhen Dou, Jiachen Lu, Weihan Sun, Haifeng Chen</i>	
Improving the Continuity and Smoothness of the Compact Model for Organic Light-Emitting Diode	54
<i>Wenbin Wang, Cong Li, Haokun Li, Xiaoming Li, Shaoxi Wang, Hailong You</i>	
Automatic Standard Cell Layout Generator Integrated with Design Expertise	59
<i>Yuan Lei, Chenyue Ma, Beiping Yan</i>	
Impacts of Parasitic Effects on PCM-based Neuromorphic Circuits under Advanced Technology Nodes	64
<i>Xiaobao Zhu, Baokang Peng, Feilong Ding, Ziyu Xie, Yihan Chen, Lining Zhang</i>	
Virtual Fab Coupled Physics-Based Simulation Design of sub-2nm Node 3D Heterogeneous Si/IGZO 6T SRAM	69
<i>Zhaohai Di, Yue Zhao, Yanna Luo, Haoqing Xu, Lingfei Wang, Jianhui Bu, Yongliang Li, Zhenhua Wu</i>	
Optimization of Breakdown Characteristic for SiC MOSFETs by Self-developed Simulator	74
<i>Yuanzhao Hu, Fei Liu, Xiaoyan Liu</i>	
A New Framework to MOS Device for Cryogenic Application: Linking Materials with Modeling	79
<i>Chenyang Zhang, Maokun Wu, Miaoqia Yuan, Yongkang Xue, Pengpeng Ren, Runsheng Wang, Zhigang Ji</i>	
Simulation of MEMS Microfabrication Process Based on Narrow Band Level Set and Ray Tracing Methods	84
<i>Bin-Bin Zheng, Zai-Fa Zhou, Ji-Yang Liu, Su-Xin Bao, Qing-An Huang</i>	
A Neural Network-based Framework for Accelerated Device-Circuit Electrothermal Co-Simulations in GAAFETs.....	89
<i>Hengyi Liu, Sihao Chen, Wu Dai, Yu Li, Baokang Peng, Lining Zhang, Runsheng Wang, Ru Huang</i>	
❖ Chapter 2: Analog Circuit	
A Parallel Acceleration Technique based on Bordered Block Diagonal Matrix Reordering for Exponential Integrator Method	94
<i>Hang Zhou, Dongen Yang, Yangfei Lin, Yong Dai, Quan Chen</i>	
Automated Generation Procedure for Fully Differential Op-amp Using TED	100
<i>Yuefan Wang, Qingsen Wu, Yuan Wang, Qian Qin, Jinglei Hao, Chenkai Chai, Yukai Lu, Jiwen Huang, Lin Li, Zuochang Ye</i>	
A Novel Automatic Placement Generation Tool for Current Mirror in Analog Circuits	106
<i>Yuejiao Wang, Lining Wang, Bijian Lan, Jing Wan</i>	
Design and Implementation of the MTP Compiler	112
<i>Yuan Zhao, Yunlong He, Jianhao Xiao, Zhongbo He, Zuochang Ye, Yan Wang</i>	

HD-MCTS: An Analog Circuit Optimization Algorithm Based on High-dimensional Monte Carlo Tree Search	118
<i>Zhao Yiyang, Lemeng Li, Ruiyu Lyv, Zhaori Bi, Changhao Yan, Xuan Zeng</i>	
P-TICER: An Effective Parallel TICER Acceleration Method for Model Order Reduction	125
<i>Zijia Zhang, Dan Niu, Zhou Jin, Pengju Chen, Zhenya Zhou, Changyin Sun</i>	
A Subcircuit Matching Approach to Structural Analog Circuit Model Generation and Sizing	131
<i>Xisheng Zhang, Mingzhen Li, Qixu Xie, Guoyong Shi</i>	
KIDEA: A Novel Multi-Objective Optimization Algorithm and its application in Analog Circuit Design.....	137
<i>WenZhao Sun, WangGe Zuo, Bijian Lan, Qing Peng, LiQian Zhang, Jing Wan</i>	
An Efficient Approach to Multiphase Constant On-Time Buck Converter Simulation.....	143
<i>Xianting Lu, Xunzhao Yin, Cheng Zhuo</i>	
Hierarchical Optimization based on Partial Performance Tradeoff Modeling Method for Large Scale Analog Circuits	149
<i>Xinyu Yu</i>	
CGAT-TICER: A Compressed GAT-based TICER for RC Reduction	155
<i>Yuchao Zhong, Yunfan Zuo, Leyun Tian, Sen Hu, Hao Yan</i>	
Routing Generative Pre-Trained Transformers for Printed Circuit Board.....	160
<i>Hao Wang, Jun Tu, Shenglong Bai, Jie Zheng, Weikang Qian, Jienan Chen</i>	
Topology Optimization of Operational Amplifiers Using A Performance-aware Representation	166
<i>Jinyi Shen, Fan Yang, Li Shang, Changhao Yan, Zhaori Bi, Dian Zhou, Xuan Zeng</i>	
Automated Design of a Strong-ARM Dynamic Comparator.....	171
<i>Jiaquan Jiang, Qingsen Wu, Yuan Wang, Qian Qin, Jinglei Hao, Chenkai Chai, Yukai Lu, Jiwen Huang, Lin Li, Zuochang Ye</i>	
RLCkt II: Deep Reinforcement Learning via Attention-Aware Sampling for Analog Integrated Circuit Transistor Sizing Automation.....	177
<i>Wangge Zuo, WenZhao Sun, Bijian Lan, Jing Wan</i>	
Implementation of Mixed Precision Sparse Matrix Solving in the Large Scale Circuit Transient Simulation	182
<i>Jingrui Chen, Minghou Cheng, Xuan Xiao, Xiaomeng Jiao, Jinyu Zhang, Xiaolue Lai, Zhenya Zhou</i>	
Automated Design of Analog Circuits Based on Parallel Trust Region Bayesian Optimization	187
<i>Peng Dong, Ruiyu Lyu, Chunxi Wang, Jiale Chen, Linfeng Jiang, Cunqing Lan, Zhaori Bi, Changhao Yan</i>	
High-Dimensional Analog Circuit Sizing via Bayesian Optimization in the Variational Autoencoder Enhanced Latent Space	193
<i>Wangzhen Li, Zhaori Bi, Xuan Zeng</i>	

A Wideband Behavioral Model with Multiple States for RF Power Amplifier Based on Improved Recurrent Neural Network.....	198
<i>Xingyu Tang, Zhikai Wang, Yan Wang</i>	
❖ Chapter 3: Digital Design & Verification	
How Good is Your Property? A New Metric for Formal Property Coverage	204
<i>Qianwen Zhao, Hongce Zhang</i>	
PWL-Explorer: A Reconfigurable Architecture for Nonlinear Activation Function with Automatic DSE	210
<i>Yiqing Mao, Huizhen Kuang, Wai-Shing Luk, Lingli Wang</i>	
Revisit Reconvergence Issue in Simulation-based Observability and Testability, and Its Rectification.....	216
<i>Feng Shi, Yutong Yao, Nan Guan, Xinjie Gao, Xiaotian Su, Nan Zhang, Zhipeng Liu</i>	
An Efficient Circuit Matching Algorithm Based on Hash Extraction of Features	222
<i>Qin He, Yingmeng Li</i>	
An Energy-efficient Multiplier Using Hybrid Approximate Logic Synthesis for Mixed-quantization CNNs....	229
<i>Yang Zhang, Qingwen Wei, Hao Cai, Bo Liu</i>	
On Accelerating Domain-Specific MC-TS with Knowledge Retention and Efficient Parallelization for Logic Optimization	235
<i>Cunqing Lan, Xinyao Wang, Zijian Jiang, Hongyang Pan, Keren Zhu, Zhaori Bi, Changhao Yan, Xuan Zeng</i>	
Towards Evaluating SEU Type Soft Error Effects with Graph Attention Network.....	241
<i>Zhangyu Li, Tun Li, Chang Liu, Liang Wang, Chunxue Liu, Yang Guo, Wanxia Qu</i>	
TLED: Training-Based Approximate Layer Exploration in DNNs with Efficient Multipliers	247
<i>Kunlong Li, Zhen Li, Lingli Wang</i>	
Automated Python-to-RTL Transformation and Optimization for Neural Network Acceleration	253
<i>Chen Yang, Renjing Hou, Qirui Yang, Wenjian Yu, Kang Zhao</i>	
GraphRTL: an Agile Design Framework of RTL Code from Data Flow Graphs	259
<i>Yuheng Qiao, Cai Xie, Zhaoting Ou, Peizhi Lei, Yan Tian, Jienan Chen</i>	
Exact Synthesis and Inversion Optimization for 3-input Resistive Majority based Logic-in-Memory	266
<i>Ming Yan, Guanghai Dong, Yong Xiao, Yun Shao, Zhufei Chu</i>	
CPGPUSim: A Multi-dimensional Parallel Acceleration Framework for RTL Simulation	272
<i>Xi Tian, Cheng Yue, Yan Pi, Tun Li, Wanxia Qu</i>	
Array Partitioning Method for Streaming Dataflow Optimization in High-level Synthesis.....	278
<i>Renjing Hou, Jianwang Zhai, Yajun Wang, Zhe Lin, Kang Zhao</i>	

Multi-dimensional Acceleration of Fault Simulation on ARM Multicore CPU.....	283
<i>Yonghao Wang, Zhiteng Chao, Senlin Wang, Feng Gu, Tiancheng Wang, Jing Ye, Huawei Li</i>	
Enhancing ASIC Technology Mapping via Parallel Supergate Computing	289
<i>Ye Cai, Zonglin Yang, Liwei Ni, Biwei Xie, Xingquan Li</i>	
A Topology-Flattening-Based Automated Incremental Synthesis Method	295
<i>Xiangli Chen, Gang Chen</i>	
TBPart: An Effective Topological Order Balanced Hypergraph Partitioning Algorithm for VLSI Processor-based Hardware Emulation.....	300
<i>Jing Tang, Shunyang Bi, Haonan Wu, Hailong You</i>	
A Novel Structural Choices Generation Method for Logic Restructuring	306
<i>Zhang Hu, Chengyu Ma, Zhufei Chu</i>	
A Logic Optimization Method Using Reinforcement Learning	312
<i>Yuting Cai, Yue Wu, Xiaoyan Yang, Zhufei Chu</i>	
Automatic Multi-Parameter Tuning for Logic Synthesis with Reinforcement Learning.....	318
<i>Zhenghao Cui, Minghua Shen</i>	
System Routing and TDM Assignment Optimization in Multi-2.5D FPGA-Based Prototyping Systems	324
<i>Chenxi Huang, Pengfei Chu, Shunyang Bi, Richard Sun, Hailong You</i>	
Multiplication Complexity Optimization based on Quantified Boolean Formulas	332
<i>Jun Zhu, Hongyang Pan, Zhufei Chu</i>	
OhmNet: General Static IR Drop Estimation Neural Network Architecture.....	337
<i>Mingbo Hao, Junyi Qian, Zhiting Li, Zhangrui Qian, Weiwei Shan</i>	
Towards Smart Industrial Hardware Formal Verification.....	343
<i>Hui-Ling Zhen, Shixiong Kai, Lihao Yin, Haoyang Li, Min Li, Zhentao Tang, Junhua Huang, Yingzhao Lian, Mingxuan Yuan, Yu Huang</i>	
Efficient Verification Framework for RISC-V Instruction Extensions with FPGA Acceleration.....	345
<i>Zijian Jiang, Keran Zheng, Yungang Bao, Kan Shi</i>	
AIP-SEM: An Efficient ML-Boost In-Place Soft Error Mitigation Method for SRAM-based FPGA.....	351
<i>Zhuoli Wang, Lei Chen, Shuo Wang, Jing Zhou, Chunsheng Tian, Hanxu Feng</i>	
DUET: FPGA-Accelerated Differential Testing Framework for Efficient Processor Verification.....	355
<i>Shoulin Zhang, Ziqing Zhang, Yungang Bao, Kan Shi</i>	
A General Framework for Efficient Logic Synthesis.....	361
<i>Lei Chen, Xing Li, Tsaras Dimitrios, Zhihai Wang, Yinqi Bai, Mingxuan Yuan</i>	

❖ Chapter 4: Physical Implementation

Detailed-Routability-Driven Global Routing with Lagrangian-Based Rip-up and Rerouting.....	363
<i>Junkang Jiang, Pengju Yao, Wenxing Zhu</i>	
Effective Heterogeneous Graph Neural Network for Routing Congestion Prediction	369
<i>Zhongdong Qi, Qi Peng, Shizhe Hu, Hailong You</i>	
OpenPARF 3.0: Robust Multi-Electrostatics Based FPGA Macro Placement Considering Cascaded Macros Groups and Fence Regions.....	374
<i>Jing Mai, Jiarui Wang, Yifan Chen, Zizheng Guo, Xun Jiang, Yun Liang, Yibo Lin</i>	
LoopRoute: A Fast and Efficient Routing Method for Die-to-Die UCIe Interconnections	380
<i>Weiying Ji, Haochang Tian, Fei Li, Hailong Yao</i>	
Simultaneous Escape Routing Algorithm for Large-scale Pin Arrays	386
<i>Ze Yang, Kunwei Hu, Qinghai Liu, Jiarui Chen</i>	
Differentiable Rectilinear Steiner Trees for Analytical Placement.....	392
<i>Zhiyang Chen, Hailong Yao, Tsung-Yi Ho, Ulf Schlichtmann, Xia Yin</i>	
Static Timing Analysis Acceleration to Attack Process Corner Explosion by Matrix Filling Prediction.....	398
<i>Longze Wang, Zhelong Wang, Wei X. Xing, Ning Xu, Yuanqing Cheng</i>	
Edge Pair-Based Layout Pattern Matching using Space-filling Curve	404
<i>Qingsheng Qiu, Yuqing Zhang, Wuxin Ge, Chao Wang</i>	
Fast Electromigration Stress Evolution Analysis Based on Relative Gain Array.....	410
<i>Zixuan Meng, Xiaoman Yang, Yuhan Zhang, Wenjie Zhu, Tianshu Hou, Hai-Bao Chen</i>	
An Efficient Statistical Clock Skew Analysis Method for Clock Trees	416
<i>Ziyin Cui, Tao Zhang, Yihui Cai, Peng Cao, Ting-Jung Lin, Lei He</i>	
PCT-Cap: Point Cloud Transformer for Accurate 3D Capacitance Extraction	421
<i>Ye Cai, Yuyao Liang, Zhipeng Luo, Biwei Xie, Xingquan Li</i>	
Aging-aware Path Timing Prediction via Graph Representation Learning.....	427
<i>Shuhao Jia, Chuanfang Jiang, Huan Liang, Jitao Yu, Aiguo Bu</i>	
PatRouter: An Optimal-Pattern-Oriented Routability-driven Routing Algorithm for FPGA	433
<i>Chen Wu, Xuhui Li, Qiang Wang</i>	
UCMNet: Static IR Drop Estimation Using Attention Convolutional Network.....	439
<i>Jitao Yu, Huan Liang, Shuhao Jia, Chuanfang Jiang, Aiguo Bu</i>	
An Efficient Grouping Algorithm with Build-in-self-Test for Multiple Memories.....	444
<i>Zhixing Liu, Jielin Xu, Jing Tang, Song Yang, Hailong You</i>	

Effective Legalization with Cell Version Replacement for Hybrid-Row-Height Circuit Designs	450
<i>Hong Liu, Xiqiong Bai, Ziran Zhu</i>	
Multi-Strategy Bus Deviation-Driven Layer Assignment Algorithm	456
<i>Yantao Yu, Zepeng Li, Jiarui Chen, Xing Huang, Genggeng Liu, Ning Xu</i>	
A Graph AutoEncoder Approach for Fault Prediction in Test Pattern Generation	462
<i>Hongfan Zhao, Fan Yang, Jianyuan Shan</i>	
Subgraph Matching with Diversity Handling and Its Applications to PCB Placement	468
<i>Chuangdong Chen, Haiming Lin, Miaodi Su, Huan He, Jianli Chen, Ziran Zhu</i>	
An Efficient Aged Timing Analysis Method for Digital Integrated Circuit under NBTI Effect	474
<i>Yang Zhang, Zhengguang Tang, Yawei Jin, Hong Zhang, Yongsheng Sun, Chen Chen, Xiaoling Lin, Cong Li, Hailong You</i>	
Aging-aware Logic Restructure Acceleration based on Heterogeneous Graph Learning	480
<i>Zun Xue, Yuchen Liu, Yuyang Ye, Tinghuan Chen, Hao Yan, Longxing Shi</i>	
An Efficient Grouping Method for Large-Scale MBIST	486
<i>Rongjie Yang, Zheng Wang, Minghua Shen</i>	
EMGA: An Evolutionary Memory Grouping Algorithm for MBIST	492
<i>Yang Li, Yongqiang Duan, Hao Zhang, Dan Niu, Xiao Wu, Zhou Jin</i>	
On Latent Defect Acceleration	498
<i>Yawei Jin, Yang Zhang, Hong Zhang, Chen Chen, Xiaoling Lin, Yongsheng Sun, Yu Huang, Cong Li, Hailong You</i>	
Electromigration based Hardware Trojan Defense in Integrated Circuit	504
<i>Binyu Yin, Linlin Cai, Haoyu Zhang, Wangyong Chen</i>	
UnetPro: Combining Attention with Skip Connection in Unet for Efficient IR Drop Prediction.....	510
<i>Zhengfei Qi, Wanchao Wang, Chengxuan Yu, Dan Niu, Xiao Wu, Zhou Jin</i>	
Cross-die Optimization for Logic-on-Memory Face-to-Face Bonding 3-D IC Designs.....	516
<i>Siyuan Xu, Hongzhong Wu, Mingxuan Yuan</i>	
SD-SSTA: Statistical Static Time Analysis Algorithm Considering Skewed Distribution	518
<i>Fuxing Deng, Yihang Feng, Dan Niu, Xiao Wu, Zhou Jin</i>	
❖ Chapter 5: Wafer Manufacturing	
End-to-end Lithography Modeling Based on Process Parameters and Deep Learning	524
<i>Zebang Lin, Kun Ren, Dawei Gao, Yongyu Wu, Shibin Xu, Miaomiao Lu</i>	
Utilizing Neural Networks for Automated Construction of Semi-Physical CMP Models	530
<i>Qian Yue, Chen Lan</i>	

Inverse Lithography with Structured Sub-Resolution Assist Features	535
<i>Xiaoxuan Liu, Jiale Liu, Wenjing He, Yaojun Du, Li Xie, Yijiang Shen, Hong Chen</i>	
Application of a CFD Simulation on Spin Coating Process	540
<i>Xinchang Wang, Yun Wang, Yansong Liu, Yayi Wei, Tianchun Ye</i>	
An Efficient SRAM Yield Analysis Method using Multi-Fidelity Neural Network	547
<i>Zhongxi Guo, Weihan Sun, Ziqi Wang, Yihui Cai, Longxing Shi</i>	
RLIF-Net: Unsupervised Trace-SPC Fault Detection Solution Based on Representation Learning and Isolation Forest.....	552
<i>Haixiang Qiu, Hui Jiang</i>	
Uncertainty Quantitative Analysis of MEMS Sensors Based on Physical Guided Deep Learning	558
<i>Yifan Zhang, Wenxin Zhang, Zikun Ni, Linfeng Zhao, Zaifa Zhou</i>	
Budget Analysis of Multiple Parameters in EUV Lithography System Based on Support Vector Machine	563
<i>Jiashuo Wang, Xiaojing Su, Yayi Wei</i>	
Model-based OPC Extension in OpenILT	568
<i>Su Zheng, Gang Xiao, Ge Yan, Meng Dong, Yao Li, Hong Chen, Yuzhe Ma, Bei Yu, Martin Wong</i>	
A Fast Imaging Model of Plasmonic Lithography for Line/space Patterns Based on Parameter Sweep	574
<i>Huwen Ding, Yayi Wei</i>	
Line Edge Roughness Modeling for Continuous Time-space Resist Simulations.....	579
<i>Hong Chen, Li Xie, Lijie Wei, Zhong Shu, Binglin Qiu, Zhuoran Pei, Geng Bai</i>	
Adaptive Time-stepping Method for CMP Simulation Efficiency	587
<i>Rui Zhang, Yu-wei Xie, Qing Zhang, Huan Kan, Wei-wei Pan</i>	
Performance Analysis of Different Processor Architectures Applied to CMP Process Modeling Acceleration	592
<i>Zhirui Niu, Yan Sun, Qin Du, Lan Chen</i>	
❖ Chapter 6: Packaging & Multi-Physics	
Study on Compact Thermal Model for 3D Interlayer Electronic Cooling based on Fluid-Solid Coupling Heat Transfer.....	600
<i>Zhizhu Cao, Jun Tao, Run Xu, Jiming Li, Yu Chen</i>	
Chiplet Placement Order Exploration Based on Learning to Rank with Graph Representation	605
<i>Zhihui Deng, Yuanyuan Duan, Leilai Shao, Xiaolei Zhu</i>	
An Equivalent Circuit Model for Elliptic Cylindrical TSV Considering the Temperature Influence	611
<i>Wenbo Guan, Xiaoyan Tang, Hongliang Lu, Jingru Tan, Yuming Zhang, Yimen Zhang</i>	

ATSim3D: Towards Accurate Thermal Simulator for Heterogeneous 3D-IC Systems Considering Nonlinear Leakage and Conductivity	618
<i>Qipan Wang, Tianxiang Zhu, Yibo Lin, Runsheng Wang, Ru Huang</i>	
Domain Decomposition and Reduction Method for Efficient Thermal Simulation and Design of 2.5D Heterogeneous Integration	624
<i>Shunxiang Lan, Min Tang, Junfa Mao</i>	
Design and Optimization of Water Droplet Interconnect Structures for Millimeter-Wave Band Applications	628
<i>Ruixin Liu, Junqin Zhang, Cong Wei, Guangbao Shan</i>	
Rectangular Approximation for Curved-Shape Power Density in Chip Thermal Analysis	632
<i>Ao Wang, Luqiao Yin, Wenxing Zhu, Aiyong Guo, Jingjing Liu, Min Tang, Liang Chen, Jianhua Zhang</i>	
Hybrid Model-Based Thermal Analysis Methodology for Integrated Circuits	637
<i>Kexin Zhu, Runjie Zhang, Qing He</i>	
❖ Chapter 7: Emerging Technologies	
CAPEDL: Cycle-Accurate Power Estimation with Deep Learning	642
<i>Tong Liu, Haoyu Zhao, Yangdi Lyu</i>	
A Lightweight Inception Boosted U-Net Neural Network for Routability Prediction	648
<i>Hailiang Li, Yan Huo, Yan Wang, Xu Yang, Miaohui Hao, Xiao Wang</i>	
Fast Design Technology Co-Optimization Framework for Emerging Technology with Hierarchical Graph Embedding	654
<i>Tianliang Ma, Guangxi Fan, Xuguang Sun, Zhihui Deng, Kain lu Low, Leilai Shao</i>	
FormalEval: A Method for Automatic Evaluation of Code Generation via Large Language Models	660
<i>Sichao Yang, Ye Yang</i>	
Model Inference Optimization on ReRAM-Based Accelerators with Intra- and Inter-OU Similarity	666
<i>Tao Li, Qinghang Zhao</i>	
ERL-LS: Accelerating Primitive Sequence Generation of Logic Synthesis with Evolutionary Reinforcement Learning	672
<i>Chenyang Lv, Boning Zhang, Weikang Qian, Zhezhi He</i>	
Toward Efficient Co-Design of CNN Quantization and HW Architecture on FPGA Hybrid-Accelerator	678
<i>Yiran Zhang, Guiying Li, Bo Yuan</i>	
Knowledge Transfer for GaN HEMTs Parameter Extraction Based on Hybrid Model	684
<i>Yangbo Wei, Wei Xing, Ting-Jung Lin, Lei He</i>	
FPGA Divide-and-Conquer Placement using Deep Reinforcement Learning	690
<i>Shang Wang, Deepak Ranganatha Sastry Mamillapalli, Tianpei Yang, Matthew E. Taylor</i>	

An FPGA-based Multi-Core Overlay Processor for Transformer-based Models.....	697
<i>Shaoqiang Lu, Tiandong Zhao, Rumin Zhang, Ting-Jung Lin, Chen Wu, Lei He</i>	
A Review of DNN and GPU in Optical Proximity Correction	703
<i>Huming Zhu, Xiangyu Jiang, Delong Shu, Xinyue Cheng, Biao Hou, Hailong You</i>	
ChatChisel: Enabling Agile Hardware Design with Large Language Models.....	710
<i>Tianyang Liu, Qi Tian, Jianmin Ye, LikTung Fu, Shengchu Su, Junyan Li, Gwok-Waa Wan, Layton Zhang, Sam-Zaak Wong, Xi Wang, Jun Yang</i>	
A Survey of Reinforcement Learning for Electronic Design Automation	717
<i>Huming Zhu, Xiangru Chen</i>	
An FPGA-based Efficient Streaming Vector Processing Engine for Transformer-based Models.....	722
<i>Zicheng He, Tiandong Zhao, Siyuan Miao, Chen Wu, Lei He</i>	
GOMARL: Global Optimization of Multiplier using Multi-Agent Reinforcement Learning.....	728
<i>Yi Feng, Chao Wang</i>	
❖ Chapter 8: Miscellaneous	
An Open-Source Tool to Model and Explore Complex Routing Architecture for FPGA	734
<i>Kaichuang Shi, Lingli Wang</i>	
A High Critical Charge 16T Soft-Error-Aware SRAM for Aerospace Applications.....	740
<i>Na Bai, Wenhao Zhu, Xinjie Zhou, Yaohua Xu, Yi Wang</i>	
SATGL: An Open-source Graph Learning Toolkit for Boolean Satisfiability	746
<i>HongTao Cheng, Jiawei Liu, Jianwang Zhai, Mingyu Zhao, Cheng Yang, Chuan Shi</i>	
FlattenRTL: An Open Source Tool for Flattening Verilog Module at RTL Level	752
<i>Xiangchen Meng, Ziyue Zheng, Yangdi Lyu</i>	
❖ Poster	
Contour Extraction Assists in Distinguishing Lithographic Hotspot.....	758
<i>Liuye Meng, Kun Ren, Dawei Gao, Yongyu Wu</i>	
Parallel DGTD Algorithm with LTS Scheme for Electrical Large Problems Based on Supercomputer	760
<i>Wenhao Liu, Liang Chen, Ping Li</i>	
Learning Peak Temperature in 3DICs by Deep Differentiable Forest	761
<i>Yingshi Chen, Min Zhu, Xueyin Zhang, Yusheng Zhai, Chunyang Feng</i>	
Pattern Match in VLSI Layout with Window Dance	763
<i>Zhiping Mou, Kun Ren, Dawei Gao, Shibin Xu</i>	

A GPU-Accelerated Harmonic Balance Method for Nonlinear Radio-Frequency Circuit Simulation.....	764
<i>Zhengzhuo Wang, Yanliang Sha, Lingyun Ouyang, Quan Chen, Jianguo Hu, Deming Wang</i>	
A High-precision De-embedding Method for GaAs IPD Wafer-level Testing.....	765
<i>Ma Lingmei, Song Xiaotian, Christine Tan, Yao Wei, Qian Rong, Wu Liang</i>	
Research on Thermal Resistance Matrix of Multi-chip Module Based on Aluminum Nitride Ceramic Substrate	768
<i>Zhanqi Zhu, Junqin Zhang, Renhao Song, Guangbao Shan</i>	
A Relative-Priority Encoding Genetic Algorithm for Integrated Mapping and Scheduling Optimization	770
<i>Zhifang Sun, Shengjie Jin, Jinxue Duan, Junqiang Jiang, Zebo Peng</i>	
CDE: A Novel CGRA Development Environment with Fast Design Space Exploration Framework	772
<i>Sichao Chen, Yuan Dai, Jide Zhang, Huizhen Kuang, Xuchen Gao, Wai-Shing Luk, Wenbo Yin, Lingli Wang</i>	
Co-optimization of Circuit Aging and Thermal Resilience: Buffer Insertion and Gate Sizing	773
<i>Ling Xiong, Wangyong Chen, Mingyue Zheng, Linlin Cai</i>	
An Innovative and Efficient Unified Analysis Model for AlGaN/GaN HEMTs.....	775
<i>Baoqin Zhang, Junjie Feng, Yujie Han, Chuanzhong Xu, Fei Yu, Shuting Cai</i>	
Framework Independent Modeling for SRAM-Based In-Memory Computing.....	777
<i>Sicun Li, Ning Zhang, Wenbo Zhang, Runhua Yang, Yuchun Chang, Botao Xiong</i>	
Automatic Adder Tree Re-Synthesis Tool for Digital Compute-in-Memory Low-power Optimization	778
<i>Wencong Wu, Shasha Guo, Hongyi Zhang, Xuxia Zhong, Chengchen Wang, Haozhe Zhu, Haidong Tian, Xiaoyang Zeng, Chixiao Chen</i>	
Neural Network-based Classification of Breakdown Mechanisms and Prediction of breakdown Voltage and On-resistance for 4H-SiC Trench Gate MOS Devices.....	780
<i>Jiayi Zhang, Shiyang Zhang, Ze Sun, Yucheng Wang, Yupan Wu, Wei Li, Shaoxi Wang</i>	
Single Event Upset and Radiation Hardening of the Complementary FET (CFET) based 6T-SRAM	782
<i>Zhengxin Zhang, Wangyong Chen, Jianwen Lin, Linlin Cai</i>	
The Hypergraph Partitioning Benchmark Suite	783
<i>Fang Zhang, Liyan Yu, Shunyang Bi, Pengfei Chu, Jing Tang, Hailong You</i>	
❖ Invited Paper	
Functional Safety and Reliability of Interconnects throughout the Silicon Life Cycle.....	785
<i>Sybille Hellebrand, Somayeh Sadeghi-Kohan, Hans-Joachim Wunderlich</i>	
Security-Aware Design of Cyber-Physical Systems for Control over the Cloud	786
<i>Zebo Peng</i>	

Robust Test of Small Delay Faults under PVT-Variations.....	787
<i>Hans-Joachim Wunderlich, Hanieh Jafarzadeh, Sybille Hellebrand</i>	
HT-TMR: An Efficient Netlist-Level TMR Tool for FPGA SEU Mitigation.....	788
<i>Yaowei Zhang, Lei Chen, Shuo Wang, Jing Zhou, Chunsheng Tian, Yu Li, Yuanhang Bu, Yuxin Yu</i>	
AiEDA: An Open-source AI-native EDA Library.....	794
<i>Zhipeng Huang, Zengrong Huang, Simin Tao, Shijian Chen, Zhisheng Zeng, Liwei Ni, Chunan Zhuang, Weiguo Li, Xueyan Zhao, He Liu, Biwei Xie, Xingquan Li</i>	
A Security-Driven FPGA Application Development Workflow Based on GCN Algorithm	796
<i>Ke Xiao, Lei Chen, Yanlong Zhang, Shuo Wang, Jing Zhou, Xueting Zhang, Shuang Jiang</i>	

Author Index