

2024 IEEE 4th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA 2024)

**Bangalore, India
17-18 May 2024**



**IEEE Catalog Number: CFP2484Z-POD
ISBN: 979-8-3503-6227-5**

**Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP2484Z-POD
ISBN (Print-On-Demand):	979-8-3503-6227-5
ISBN (Online):	979-8-3503-6226-8

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

FPGA Accelerated Convolutional Neural Network for Detection of Cardiac Arrhythmia	1
<i>Soumyashree Mangaraj, Pawan Oraon, Samit Ari, Ayas Kanta Swain, Kamalakanta Mahapatra</i>	
Pulsed Latch Based Pipelined LFSR for Cybersecurity Applications	7
<i>Sidhaarthi Patil, Vaishnavi B V, Shreya Gangadhara, Sahil Naik, Sunita M S</i>	
A Modular Multilevel Derived Converter with a Robust and Dynamic Sliding Mode Control for Electric Vehicles	12
<i>Aaron Celestine Prakash, Shreesh Sakshya Bajpai, Vaishnav Mohan, Sudeendra Kumar K</i>	
Design of Spin-FET Electrical Model for Basic Gates.....	18
<i>Priti Jagatsing Rajput, Sheetal U. Bhandari, Deepti Khurje</i>	
Analyzing the Low Power Techniques in SRAM Cells at 45nm Node Technology.....	23
<i>Sandeep Dhariwal, Aby K Thomas, Reeba Korah, Manasi S</i>	
Performance of Well-Organized VLSI Architecture for Three Operand Binary Adder	28
<i>Essaki Baveth M, Siva Arumugam R, Kumaravel Ravi V, Vivek Anand I</i>	
A Low-Complexity Design for Complex Multiplication Using Radix-4 Booth Encoding.....	33
<i>Anil Kali, B. S. Khuntia, S. L. Sabat, P. K. Meher</i>	
Performance Comparison of 2 X1 Multiplexer Based High Performance Static and Dynamic Nanoscale Carry Select Adder for Future DSP Applications.....	38
<i>Ruchitha Pateru, J. Ajayan, Korutla Alekhya, Gunde Vamshi, Jannu Ruthvik, Shashank Rebelli</i>	
A Mathematical Model of TiO ₂ Memristor Without Control Parameters	43
<i>Sara Paul, R. K. Kavitha</i>	
Test Power Optimization Using Power Gating Techniques.....	48
<i>Adarsh S, Ashwin Sebastian Davison, Abhijna N, Fazia N, Niju Rajan</i>	
Power Efficient Hybrid Low-Power Technique for an SRAM Cell	54
<i>Rahul Sai Srinivas P, Shamik Chakraborty, Lalitha S</i>	
Route Critical Nets in Upper Layers to Fix Timing Issues in Block Level CTS.....	60
<i>Raja Krishnamoorthy, M. Irshad Ahamed, Polisetty Balaji, Chenepalli Bharath Kumar Reddy, Kadiveti Penchala Reddy, Surya Kiran</i>	
Circuit Techniques for High Performance in CDDK Domino Logic	65
<i>V Arun, Himanshu Kumar, H Sasipriya P, Anita Angeline A</i>	
Adaptive Leaky-Integrate-And-Fire Neuron Model Design and Analysis	69
<i>Arnab Deb, David Selvakumar</i>	
Power Estimation of Digital VLSI Circuits Using Machine Learning	75
<i>Manish I. Patel, Srushti Patel</i>	
High Speed Fault Tolerant Approximate Adder for Low Power Application.....	79
<i>Parishmita Goswami, Rakesh Biswas</i>	

Deep Learning Based Graph Neural Network Technique for Hardware Trojan Detection at Register Transfer Level	84
<i>Anindita Chattopadhyay, Siddharth Bisariya, Anantram Patel, Sowmya Sunkara, Vijay Kumar Sutrakar</i>	
Enhanced Electrochemical Properties of Fe Doped TiO ₂ Nanotubes for Supercapacitor Application	89
<i>Sarda Sharma, Sandeep Singh Chauhan, Karumbaiah N. Chappanda</i>	
Quantum-Enhanced Deep Q Learning with Parametrized Quantum Circuit.....	93
<i>Manjunath T D, Biswajit Bhowmik</i>	
LR-Based Performance Evaluation of MoCs	99
<i>Pallabi Hazarika, Biswajit Bhowmik</i>	
Analysis of Selected Load Balancing Algorithms in Containerized Cloud Environment for Microservices	105
<i>Divarshana Saxena, Biswajit Bhowmik</i>	
A 5GHz Gain-Bandwidth Op-Amp in 180nm CMOS Technology	111
<i>Munzir Reza, Ayush Sharma, Afzal Malik, Mohsin Hussain, Naushad Alam, G S Javed</i>	
FPGA Realization of High-Efficient Address Generator Algorithm for WiMAX Deinterleaver	115
<i>Veera Boopathy E, Kalirajan K, Mohamed Kasim S, Muges A, Rathish S G, Nithyaganesh S, Vimalraj P</i>	
Design and Implementation of an Efficient 32-Bit Fixed-Point Newton-Raphson Division-Based Reciprocal Computing Unit.....	120
<i>Chiranthgynan S Aragula, Budi Preethi, Chinthala Ramesh</i>	
Analysis of Different LFSRs for VLSI IC Testing	126
<i>Shubham Gupta, Garima Goyal, Ashwani Kumar Rana</i>	
Design and Performance Analysis of 10T SRAM Cell Using Dopingless Vertical Nanowire Tunnel FET with NC Effect.....	131
<i>Anjana Bhardwaj, Pradeep Kumar, Balwinder Raj</i>	
Dual Obfuscation Techniques for DSP Based Circuits.....	137
<i>Harpitha Yadav P, Kasthuri Shankara J, Poornachandra Radder, Thanuja B, Annapurna K Y</i>	
Impact of Clock-Gating on ALU Optimized RISC-V Microarchitectures for Low Power Applications.....	142
<i>Srujan Sathish, Prajwal N, Akshaya R, Kaustubha, Sudeendra Kumar</i>	
Towards Scalability and Performance: Framework for Heterogeneous Cluster Integration in Deep Learning Accelerators.....	148
<i>K Bhagirath, Dheeraj Pant, Abhishek Tiwari, Vivek Khaneja</i>	
VLSI Implementation of CSD Based Efficient FIR Filter for ECG Signal Denoising.....	154
<i>Prabhavathy M, Sakthivel S M</i>	
Variability in Switching Characteristics of RRAM Based 1T-1R Configuration and Memory Array	160
<i>Nivetha T, B. Bindu</i>	

Author Index