# 2024 IEEE 42nd VLSI Test Symposium (VTS 2024)

Tempe, Arizona, USA 22-24 April 2024



**IEEE Catalog Number: CFP24029-POD ISBN**:

979-8-3503-6379-1

#### Copyright © 2024 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP24029-POD

 ISBN (Print-On-Demand):
 979-8-3503-6379-1

 ISBN (Online):
 979-8-3503-6378-4

ISSN: 1093-0167

#### Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA

Phone: (845) 758-0400 Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



#### Table of Contents

A Method for Simulating Mixed-Signal ATE Tests...1
Stephen SUNTER, Vladimir ZIVKOVIC, Bartlomiej PRASELSKI

A Novel Self-referencing Approach Using Memory Power-up States for Detecting COTS SRAMs...8

Gaines ODOM, Zakia Tamanna TISHA, Ujjwal GUIN

A Storage Based LBIST Scheme for Logic Diagnosis...15 Subashini GOPALSAMY, Irith POMERANZ

Analyzing and Mitigating Circuit Aging Effects in Deep Learning Accelerators...22

Sanjay DAS, Shamik KUNDU, Anand MENON, Shubha KHAREL, Yihui REN, Kanad BASU

Analyzing the Impact of Scheduling Policies on the Reliability of GPUs running CNN operations...29

Robert LIMAS SIERRA, Francesco PESSIA, Juan GUERRERO, Josie RODRIGUEZ CONDIA, Matteo SONZA REORDA

Built in self test for RSFQ circuit...36 Mingye LI, Yunkun LIN, Sandeep GUPTA

Calibration and Source Localization Using an Array of Resistive Metal Oxide Gas Sensors...43

Ishaan BASSI, Sule OZEV

Characterization of 14nm CMOS Technology At Cryogenic Temperatures Using Dense Addressable Arrays...50

Raphael ROBERTAZZI, David FRANK, John TIMMERWILKE, Kevin TIEN, Peilin SONG, Daniel FRIEDMAN

Customizing ATPG User-Defined Stresses and Tests To Target Cell-Neighborhood-Bridging Defects...57

Stephen TRAYNOR, Saidapet RAMESH, Lawrence HERR, Maryfe HERNANDEZ, Scott CHEN

Drop-Connect as a Fault-Tolerance Approach for RRAM-based Deep Neural Network Accelerators...62

Mingyuan XIANG, Xuhan XIE, Pedro SAVARESE, Xin YUAN, Michael MAIRE, Yanjing LI

Enhanced Wear-Out Sensor Design in a 12nm Process for Separable Stress Regime Monitoring...69

Ian HILL, Mateo RENDÓN, Andre IVANOV

Error Resilient Hyperdimensional Computing Using Hypervector Encoding and Cross-Clustering...76

Mohamed MEJRI, Chandramouli AMARNATH, Abhijit CHATTERJEE

Evaluating the Reliability of Supervised Compression for Split Computing...83 *Juan GUERRERO, Josie RODRIGUEZ CONDIA, Marco LEVORATO, Matteo SONZA REORDA* 

Fuzz Wars: The Voltage Awakens - Voltage-Guided Blackbox Fuzzing on FPGAs...89

Kai SU, Mark Leon GIRAUD, Anne BORCHERDING, Jonas KRAUTTER, Philipp NENNINGER, Mehdi TAHOORI

Sequential Decoders for Binary Linear Block ECCs...96 *Valentin GHERMAN, Cyrille LAFFOND* 

Logic-AAA: Debug of Logic Failures with an on-ATE Expert System...101 Chris NIGH, Shawn BLANTON

Multi-Level Reference for Test Coverage Enhancement of Resistive-Based NVM...107

Sina BAKHTAVARI MAMAGHANI, Jongsin YUN, Martin KEIM, Mehdi TAHOORI

NN-ECC: Embedding Error Correction Codes in Neural Network Weight Memories using Multi-task Learning...114

Soyed Tuhin AHMED, Surendra HEMARAM, Mehdi TAHOORI

On the Sensitivity of Analog Artificial Neural Network Models to Process Variation...121

Nosheen AFROZ, Ahmad Sayeed SAYEM, Georgios VOLANIS, Dzmitry MALIUK, Haralampos STRATIGOPOULOS, Yiorgos MAKRIS

Reliability analysis and mitigation for analog computation-in-memory: from technology to application...128

Mahta MAYAHINIA, Haneen G. HEZAYYIN, Mehdi TAHOORI

Scenario-based Test Content Optimization: Scan-Test vs. System-Level Test...135

Nourhan ELHAMAWY, Jens ANDERS, Ilia POLIAN, Matthias SAUER

Static Gate-Level Information Flow for Hardware Information Security with Bounded Model Checking...142

Yiqiang ZHAO, Gongsen QU, Qizhi ZHANG, Yao LI, Zhengyang LI, Jiaji HE

Structural Built In Self Test of Analog Circuits using ON/OFF Keying and Delay Monitors...149

Suhas KRISHNA KASHYAP, Chinmaye RAGHAVENDRA, Suriyaprakash NATARAJAN, Sule OZEV

Temperature-Insensitive Soft-Error-Tolerant Flip-Flop Design For Automotive Electronics...156

Ralf E.-H. YEE, Yen-Ju SU, Lowry P.-T. WANG, Charles H.-P. WEN, Herming CHIUEH

Test Compaction Using (k,1)-Cycle Tests...163 Irith POMERANZ

Testing a Transistor-Level Programmable Fabric: Challenges and Solutions...170

Apurva JAIN, Thomas BROADFOOT, Carl SECHEN, Yiorgos MAKRIS

Testing and Fault Diagnosis for Multi-level Resistive Random-Access Memory in Monolithic 3D Integration...177

Shao-Chun HUNG, Partho BHOUMIK, Krishnendu CHAKRABARTY

Transformer and Its Variants for Identifying Good Dice in Bad Neighborhoods...184

Cheng-Che LU, Chi-Chih CHANG, Chia-Heng YEN, Shuo-Wen CHANG, Ying-Hua CHU, Kai-Chiang WU, Mango CHAO

WaferCap: Open Classification of Wafer Map Patterns using Deep Capsule Network...191

Abhishek Kumar MISHRA, Mohammad Ershad SHAIK, Anush LINGAMOORTHY, Suman KUMAR, Anup Kumar DAS, Nagarajan KANDASAMY, Nur TOUBA

Practical Considerations on ESD Testing...198

Xunyu Li, Weiquan Hao, Zijin Pan, Yunru Miao, Zijian Yue, Albert Wang

AIN Sputtering Parameter Estimation Using A Multichannel Parallel DCT Neural Network...201

Yingyi Luo, Talha M. Khan, Emadeldeen Hamdan, Xin Zhu, Hongyi Pan, Didem Ozevin, A. Enis Cetin

A High Level Synthesis Methodology for Dynamic Monitoring of FPGA ML Accelerators...206

Ryan F. Forelli, Rui Shi, Seda Ogrenci, Joshua Agar

Millimeter-wave and THz Measurement Practices...211
Saeed Zeinolabedinzadeh

Multi-Parameter Optimization of mm-Wave Antenna Layout Using Hybrid Modeling and Incremental Model Learning...215

Ferhat Can Ataman, Mohammed Aladsani, Chethan Kumar Yb, Georgios Trichopoulos, Sule Ozev

A Test Platform for Characterizing Emerging Nonvolatile Memories for Computing...220

D. Wilson, N. Gilbert, M. Spear, J. Short, C. Bennett, W. Wahby, J. Kim, R. Jacobs-Gedrim, T.P. Xiao, S. Agarwal, M. J. Marinella

Thermal Modeling and Management Challenges in Heterogenous Integration: 2.5D Chiplet Platforms and Beyond...225

Jaehyun Park, Alish Kanani, Lukas Pfromm, Harsh Sharma, Parth Solanki, Eric Tervo, Janardhan Rao Doppa, Partha Pratim Pande, Umit Y. Ogras

Overcoming Communication Bottlenecks in Scale-out Machine Learning with Silicon Photonic 2.5D Interposer Networks...229

Febin Sunny, Ebadollah Taheri, Mahdi Nikdast, Sudeep Pasricha

Test Methods for Total Ionizing Dose Effects on Capacitors...233

Chandarasekaran Ramamurthy, Harrish Anbazhagan, Rajeswara B

#### Reliability Assessment Recipes for DNN Accelerators...237

Mohammad Hasan Ahmadilivani, Alberto Bosio, Bastien Deveautour, Fernando Fernandes dos Santos, Juan-David Guerrero-Balaguera, Maksim Jenihhin, Angeliki Kritikakou, Robert Limas Sierra, Salvatore Pappalardo, Jaan Raik, Josie E. Rodriguez Condia, Matteo Sonza Reorda, Mahdi Taheri, Marcello Traiola

Addressing the Combined Effect of Transistor and Interconnect Aging in SRAM towards Silicon Lifecycle Management...248

Zhe Zhang, Mahta Mayahinia, Christian Weis, Norbert Wehn, Mehdi Tahoori, Sani Nassif, Grigor Tshagharyan, Gurgen Harutyunyan, Yervant Zorian

### Unified Functional Safety Framework for Advanced Multi-domain SoCs combining ISO 26262 & IEC61508...253

Gulroz Singh, Ankit Hegde, Vaibhav Kumar

Reliable edge machine learning hardware for scientific applications...256 *Tommaso Baldi, Javier Campos, Ben Hawks, Jennifer Ngadiuba, Nhan Tran, Daniel Diaz, Javier Duarte, Ryan Kastner, Andres Meza, Melissa Quinnan, Olivia Weng, Caleb Geniesse, Amir Gholami, Michael W. Mahoney, Vladimir Loncar, Philip Harris, Joshua Agar, Shuyu Qin* 

#### Machine Learning Based Static and Dynamic Error Calibration in Data Converters...261

Sumukh Prashant Bhanushali, Tushar Gupta, Debnath Maiti, Arindam Sanyal

#### Power-up Self Auto Calibration of High Speed SAR Converter in a 22nm FD-SOI CMOS Process...265

Vahid Rezazadehshabilouyoliya, Muhammed Mustafa Kizmaz, Ahmet Tekin

### High Precision Adaptive Calibration Feedback in RF Front-end for Digital Predistortion Application...270

Emre Ulusoy, Bahadir Ozkan, Furkan Barin, Fatih Maden, Ercem Yesil, Dursun Baran, Adem Eren, Tufan Coskun Karalar, Ahmet Tekin, Ertan Zencir

## Artificial Intelligence Based High Power Calibration Method for RF Pulse Amplifiers...275

A. Eroglu, M.N. Mahmoud

### Domain-Adapted LLMs for VLSI Design and Verification: A Case Study on Formal Verification...280

Mingjie Liu, Minwoo Kang, Ghaith Bany Hamad, Syed Suhaib, Haoxing Ren

#### CircuitOps and OpenROAD: An Infrastructure for ML EDA Research and Education...284

Vidya A. Chhabria, Wenjing Jiang, Andrew B. Kahng, Rongjian Liang, Haoxing Ren, Sachin S. Sapatnekar, Bing-Yue Wu

## LLMs for Hardware Design and Security: Boon or Bane...288 Rahul Kande, Vasudev Gohil, Matthew Delorenzo, Chen Chen, Jeyavijayan Rajendran

#### IEEE Std P3405: Standard-under-Development for Chiplet Interconnect Test/ Repair...292

Erik Jan Marinissen, Vineet Pancholi, Po-Yao Chuang, Martin Keim

### Analog Testing Technologies for Digital Exploding Societies...303

Haruo Kobayashi, Naoki Tsukahara, Keno Sato, Takashi Oshima

Silent Data Corruption...304 Shubhada Sahasrabudhe, Yervant Zorian

Test and Functional Safety Standards...305 Martin Keim, Steve Sunter, Jyotika Athavale

Al applications in test...306 Abhijit Sathaye, Sashi Obilisetty, Keith Schaub

Using AI to Address the Silicon Growth Curve...307 *Ira Leventhal, Sri Ganta, Keith Schaub* 

Yield Optimization...308 Carl Moore, John O'Donnell, Jory Twitchell

Advances on Silicon Lifecycle Reliability, Safety and Security...309
Fei Su, Jyotika Athavale, Zohaib Khan, Marc Witteman