

# **2023 IEEE International Integrated Reliability Workshop (IIRW 2023)**

**South Lake Tahoe, California, USA  
6 – 10 October 2023**



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# 2023 IEEE International Integrated Reliability Workshop (IIRW)

## PROGRAM SCHEDULE

**SUNDAY, October 8 - Please have lunch before arriving at the camp; no lunch will be served at the camp.**

- 3:00-6:00 p.m. Registration: Pick up badges, electronic handout, and attendee gift; Discussion Group and SIG Signup (*Lodge Lounge*)  
3:00-8:00 p.m. Lodge check-in: Get room assignment (prearranged) & room key (if physically challenged, please notify desk)  
6:00-7:30 p.m. DINNER (*Dining Room*)
- 7:30-8:30 p.m. **Sunday Night Tutorial** (*Angora Room*) From the Vault: Analog Electronics in Music – Francesco Maria Puglisi, *University of Modena and Reggio Emilia*  
8:30-10:30 p.m. Social (*Old Lodge*)

**MONDAY, October 9**

- 7:00-8:00 a.m. BREAKFAST (*Dining Room*)
- Plenary Session** (*Angora Room*)  
8:00-8:10 a.m. Welcome & Introduction – Francesco Maria Puglisi, *University of Modena and Reggio Emilia*  
8:10-8:20 a.m. Technical Program Overview – Charles LaRow, *Intel Corporation*  
8:20-9:20 a.m. **Keynote:** Harnessing the potential of imperfect resistive memory technologies for efficient computing – Elisa Vianello, *CEA-Leti*
- Session #1** (*Angora Room*) - **Memory**, Chair: Michael Wautl, *TU Wien*  
9:20-9:45 a.m. 1.1 Advanced Method for Predicting Lifetime of NAND Memory Data Retention Using Long term (1 Year) Characterization - Ji-seok Lee, *Samsung electronics* .....1  
9:45-10:10 a.m. 1.2 Investigating Device Degradation and Revival in Resistive Random Access Memory - Maximilian Liehr, *College of Nanoscale Science & Engineering (CNSE), SUNY Polytechnic Institute* .....5
- 10:10-10:30 a.m. Coffee and Snack Break
- 10:30-11:30 a.m. **Tutorial #1** (*Angora Room*): Emerging Memory Reliability - Cristian Zambelli, *Università degli Studi di Ferrara*  
11:30-11:55 a.m. 1.3 Analytical Model of SRAM VMin to Predict Reliability and Process Impact - Tanuj Kumar, *ST Microelectronics*  
11:55-12:00 p.m. EDS Introduction, Ravi Todi, *EDS (Angora room)* .....11
- 12:00-1:00 p.m. LUNCH (*Dining Room*)  
1:00-1:05 p.m. Announcements
- Session #2** (*Angora Room*) - **Metrology and Characterization** - Chair: Lado Filipovic, *TU Wien*  
1:05-1:40 p.m. 2.1 **Invited** Challenges for nanomaterials in the semiconductor industry of the post-nanometer era - Umberto Celano, *Arizona State University*  
1:40-2:05 p.m. 2.2 A DLTS study on Deep Trench Processing Induced Trap States in Silicon (student paper) - Paul Stampfer, *ams-OSRAM AG* .....15  
2:05-2:30 p.m. 2.3 Hot-carrier-degradation measured with charge-pumping in trench devices despite deep contacts - Sabina Susnik, *KAI GmbH* .....19
- Session #3** (*Angora Room*) - **BEOL**, Chair: James Ashton, *Keysight*  
2:30-3:05 p.m. 3.1 **Invited** Thermomigration-induced voiding in Cu interconnects - Youqi Ding, *KU Leuven and imec*  
3:05-3:30 p.m. 3.2 Ruthenium Metallization and Via Prefill for Electromigration Reliability Enhancement in Advanced Sub-3 nm Node Interconnects - *Simone Esposito, IMEC* .....23
- 3:30-3:45 p.m. Coffee and Snack Break
- 3:45-4:10 p.m. 3.3 Pulse Power Electromigration in Cu Metallization 10 Hz to 4 MHz - Mueen Mattoo, *SUNY Polytechnic* .....27  
4:10-4:45 p.m. 3.4 **Invited** Integrated Process-Mechanical Stress Analysis of 2.5D/3D ICs with Two Types of Interconnections in Advanced Packaging - Bo Ren, *ANSYS* .....32
- Session #4** (*Angora Room*) - **Transistor I**, Charles LaRow, *Intel*  
4:45-5:10 p.m. 4.1 Advanced Extraction of Trap Parameters from Single-Defect Measurements - Michael Wautl, Christian Doppler Laboratory for Single-Defect Spectroscopy at the Institute for Microelectronics, *TU Wien* .....36  
5:10-5:35 p.m. 4.2 Current Driven Modelling and SILC Investigation of Oxide Breakdown under Off-state TDDB in 28nm dedicated to RF applications - Tidjani Garba Seybou, *STMicroelectronics* .....41  
5:35-6:00 p.m. 4.3 The Major Effect of Trapped Charge on Dielectric Breakdown Dynamics and Lifetime Estimation (student paper) - Francesco Maria Puglisi, *University of Modena and Reggio Emilia* .....47

- 6:00-7:30 p.m. DINNER (*Dining Room*)
- 7:30-9:00 p.m. **Discussion Group I - Talent Pipeline from Academia to Industry** (*Cathedral Room*), Chair: Zakariae Chbili, *Intel*  
 7:30-9:00 p.m. **Discussion Group II - Challenges in Electromigration with New Materials and Constructs** (*Angora Room*), Lado Filipovic, *TU Wien*
- 9:00-10:30 p.m. Social (*Old Lodge*)

## TUESDAY, October 10

- 7:00-8:00 a.m. BREAKFAST (*Dining Room*)  
 8:00-8:10 a.m. Announcements (*Angora Room*)
- Reliability Experts Forum** (*Angora Room*)  
 8:05-9:35 a.m. **Panel #1.1: HCI** - Moderator: Zakariae Chbili, *Intel*  
 Panelist: Andreas Kerber, *Intel*  
 Panelist: Eric Bury, *Imec*  
 Panelist: Miaomiao Wang, *IBM*  
 Panelist: Minjung Jin, *Samsung*  
 Panelist: Souvik Mahapatra, *IIT Bombay*
- 9:35-10:00 a.m. Coffee and Snack Break
- 10:00-11:30 a.m. **Panel #1.2: HCI (continued)** - Moderator: Zakariae Chbili, *Intel*  
 11:30-12:00 p.m. Group Photos (*Flag Pole*)
- 12:00-1:00 p.m. LUNCH (*Dining Room*)  
 1:00-1:05 p.m. Announcements
- 1:05-2:05 p.m. **Tutorial #2** (*Angora Room*): Connecting the Dots between Analytical Magnetic Resonance Results and Semiconductor Device Reliability - Stephen Moxim, *NIST*  
 2:05-2:40 p.m. **3.5 Invited** The reliability challenges of advanced packaging - Subramanian S. Iyer, *UCLA*
- 2:40-3:00 p.m. Coffee and Snack Break
- 3:00-6:00 p.m. **Panel #2: Vmax scaling** - Moderator: Zakariae Chbili, *Intel*  
 Panelist: Bonnie Weir, *Broadcom*  
 Panelist: Jeff Hicks, *Intel*  
 Panelist: Jen-Hao Lee, *TSMC*  
 Panelist: John Faricelli, *AMD*  
 Panelist: Patrick Justison, *Globalfoundries*
- 6:00-7:30 p.m. DINNER (*Dining Room*)
- 7:30-9:00 p.m. Poster Session  
 9:00-10:30 p.m. Social (*Old Lodge*)

## WEDNESDAY, October 11

- 7:00-8:00 a.m. BREAKFAST (*Dining Room*)
- Session #5** (*Angora Room*) - **Device and Circuit**, Chair: Cristian Zambelli, *University of Ferrara*  
 8:00-8:25 a.m. 5.1 Plasma Induced Damage Test Methodology applied to a 3D Vertical NAND Memory Technology - Daniel Beckmeier, *Intel Corporation* .....54  
 8:25-8:50 a.m. 5.2 Restrictive antenna rules limiting PID degradation for MOS transistors with connected MIM-capacitors - Maximilian Feil, *Infineon Technologies AG* .....60  
 8:50-9:25 a.m. 5.3 **Invited** Reliability of Transistors based on Two-Dimensional Semiconductors - Theresia Knobloch, *TU Wien*
- 9:25-9:40 a.m. Coffee and Snack Break
- 9:40-10:15 a.m. **Tutorial #3** (*Angora Room*): From Chaos to Order: Evaluating Memristor Technologies for neural network implementations - Gennadi Bersuker, *M2D Solutions*  
 10:15-10:50 a.m. 5.4 **Invited** A Device to Circuit Framework for NBTI – Souvik Mahapatra, *IIT Bombay* .....66

- 10:50-11:15 a.m. 5.5 Reliability Analysis of RTN-based True Random Number Generators - Tommaso Zanotti, *University of Modena and Reggio Emilia* .....72
- 11:15-11:40 a.m. 5.6 Analysis of Effects of Aging on the Accuracy of Analog Computing-In-Memory Computation (*Student Paper*) - Shida Zhang, *Georgia Institute of Technology* .....78
- 11:40-12:05 p.m. 5.7 Exploring the NBTI Aging and PVT effects on RRAM-based FPGA Multiplexers Performance - Tommaso Rizzi, *IHP* .....82
- 12:05-1:05 p.m. LUNCH (*Dining Room*)
- 1:05-6:00 p.m. Open – The afternoon is free for discussion, hiking & recreation. All attendees are required to be back before dark.
- 6:00-7:30 p.m. DINNER (*Dining Room*)
- 7:30-9:00 p.m. **Discussion Group III - Aging in Advanced Nodes** (*Angora Room*), Theresia Knobloch, *TU Wien*
- 7:30-9:00 p.m. **Discussion Group IV - TDDB: Is the Power-law the end of the road?** (*Cathedral Room*), Bonnie Weir, *Broadcom*
- 9:35-10:30 a.m. Social (*Old Lodge*)

## THURSDAY, October 12

- 7:00-8:00 a.m. BREAKFAST (*Dining Room*)
- 8:00-8:05 a.m. Announcements
- Session #6** (*Angora Room*) - **Power**, Chair: Francesco Maria Puglisi, *University of Modena and Reggio Emilia*
- 8:05-8:40 a.m. 6.1 **Invited** Recent Developments in Understanding the Gate Switching Instability in Silicon Carbide MOSFETs - Maximilian Feil, *Infineon Technologies AG* .....87
- 8:40-9:05 a.m. 6.2 Unveiling the Role of Hole Barrier Traps on ON-Resistance Instability after Gate Bias Stress in p-GaN Power HEMTs - Nicolò Zagni, *University of Modena and Reggio Emilia* .....96
- 9:05-9:30 a.m. 6.3 Role of trapping/detrapping in HTRB Stress and pulsed DC conditions in AlGaIn/GaN HEMTs analyzed via TCAD simulations - Franco Ercolano, *University of Bologna* .....101
- 9:30-9:50 a.m. Coffee and Snack Break
- Session #7** (*Angora Room*) - **Transistor II**, Chair: Charles LaRow, *Intel*
- 9:50-10:25 a.m. 7.1 **Invited** Modulation of HCI in I/O analog devices Through Process Specifications - Cheikh Diouff, *STMicroelectronics* .....108
- 10:25-10:50 a.m. 7.2 On the Role of NBTI and PBTI Induced Mobility Degradation for Compact Modeling in Metal-Gate/High-k FETs (*Student Paper*) – Insaf Lahbib, *Infineon Technologies AG, TU Wien* .....116
- 10:50-11:15 a.m. 7.3 Relationship between Trapping Centers, Charge Pumping, and Leakage Currents in Hot-Carrier-Stressed Si/SiO<sub>2</sub>/HfO<sub>2</sub> Transistors – James Ashton, *Keysight* .....123
- 11:15-11:40 a.m. 7.4 Electrically active defects in Al<sub>2</sub>O<sub>3</sub>-InGaAs MOS stacks at cryogenic temperatures - Paolo La Torraca, *University of Modena and Reggio Emilia* .....127
- 11:40-11:50 p.m. Discussion Group Summary - Lado Filipovic, *TU Wien*
- 11:50-12:00 p.m. Closing Ceremony
- 12:00-1:00 p.m. LUNCH (*Dining Room*)
- 1:00 p.m. Shuttle Bus to San Francisco International Airport leaves Stanford Sierra Camp

## Poster Presentations

- RP1 Electromigration Reliability of Buried Power Rails in Vertically Stacked Devices - Lado Filipovic, *CDL for ProMod, TU Wien* .....132
- RP2 Breakdown Criteria Selection for Analyzing Advanced Node High-K TDDB Stress Data - Elijah Allridge, *Penn State University*.....N/A
- RP3 Prevention of Al Interconnect Corrosion during Temperature-Humidity-Bias (THB) Stress - Jeff Gambino, *onsemi* .....143
- RP4 Convolution neural network inference using frequency modulation in computational phase change memory - *Ahmed Trabelsi, CEA Leti* .....148
- RP5 Impact of High-K Deposition Process on the Noise Immunity of FeFETs and Their Applicability towards In-Memory-Computing - Yannick Raffel, *Fraunhofer Institute for Photonic microsystems IPMS Dresden* .....152
- RP6 On-Chip Monitoring of Time-Dependent Dielectric Breakdown (TDDB) using a Novel Leakage Current Sensor with Digital Output - Emmanuel Nti Darko, *Iowa State University* .....156
- RP7 Analyzing the Conduction Mechanism and TDDB Reliability of Antiferroelectric-like MIM Capacitors - Alison Erlene Viegas, *Fraunhofer Institute for Photonic microsystems IPMS Dresden* .....162
- RP8 Low-Frequency Noise Source and Back-Gate Coupling Effects in FDX-SOI Device - Nandakishor Yadav, *Fraunhofer Institute for Photonic microsystems IPMS Dresden* .....166
- RP9 RESET Kinetics of 28 nm Integrated ReRAM - Stefan Wiefels, *Forschungszentrum Juelich* .....170
- RP10 TID Effects on Random Telegraph Signals in Bulk 90 nm MOSFET Devices - Jereme Neuendank, *Arizona State University* .....174
- RP11 Investigation of X-ray Irradiation Impact on CeRAM - Adam Gruszecki, *UT Dallas* .....179
- RP12 Evaluation of Temperature-Humidity-Bias (THB) Robustness of 3rd Generation 650V class 4H-SiC Discrete Power MOSFET Devices - Muhammad Waseem, *Department of Electrical and Electronic Engineering at The Hong Kong Polytechnic University* .....182
- RP13 The Impact of Operation Conditions on Potentiation, Depression and Endurance Dynamics of Tantalum Oxide RRAMs - Gozde Tutuncuoglu, *Wayne State University* .....188

## Additional Papers

- On Then Absolute Sensitivity of Near-Zero Field Magnetoresistance for Device Reliability Studies - *Elijah A. Allridge*.....138