

# **2023 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2023)**

**Foz do Iguacu, Brazil  
20-23 June 2023**



**IEEE Catalog Number: CFP23179-POD  
ISBN: 979-8-3503-2770-0**

**Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP23179-POD
ISBN (Print-On-Demand):	979-8-3503-2770-0
ISBN (Online):	979-8-3503-2769-4
ISSN:	2159-3469

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## Table of Contents

A Digital SRAM Computing-in-Memory Design Utilizing Activation Unstructured Sparsity for High-Efficient DNN Inference .....	1
<i>Baiqing Zhong, Mingyu Wang, Chuanghao Zhang, Yangzhan Mai, Xiaojie Li and Zhiyi Yu</i>	
Evaluation of Digital Circuit Design by Combining Two- and Multi-Level Approximate Logic Synthesis .....	7
<i>Gabriel Ammes, Paulo Butzen, Andre Reis and Renato Ribas</i>	
tubGEMM: Energy-Efficient and Sparsity-Effective Temporal-Unary-Binary Based Matrix Multiply Unit .....	13
<i>Prabhu Vellaisamy, Harideep Nair, Joseph Finn, Manav Trivedi, Albert Chen, Anna Li, Tsung-Han Lin, Perry Wang, Shawn Blanton and John Paul Shen</i>	
Versatile Signal Distribution Networks for Scalable Placement and Routing of Field-coupled Nanocomputing Technologies.....	19
<i>Marcel Walter, Benjamin Hien and Robert Wille</i>	
Photonic Convolution Engine based on Phase-Change Materials and Stochastic Computing.....	25
<i>Raphael Cardoso, Clément Zrounba, Mohab Abdalla, Paul Jimenez, Mauricio Gomes de Queiroz, Benoit Charbonnier, Fabio Pavanello, Ian O'Connor and Sebastien Le Beux</i>	
Robustness and Power Efficiency in Spin-Orbit Torque-Based Probabilistic Logic Circuits.	31
<i>Kamal Danouchi, Guillaume Prenat, Philippe Talatchian, Louis Hutin and Lorena Anghel</i>	
A Compact Ferroelectric 2T-(n+1)C Cell to Implement AND-OR Logic in Memory.....	37
<i>Yi Xiao, Yixin Xu, Shan Deng, Zijian Zhao, Sumitha George, Kai Ni and Vijaykrishnan Narayanan</i>	
Federated Learning with Spiking Neural Networks in Heterogeneous Systems .....	43
<i>Sadia Anjum Tumpa, Sonali Singh, Md Fahim Fayal Khan, Mahmut Taylan Kandemir, Vijaykrishnan Narayanan and Chita R. Das</i>	
Fe-GCN: A 3D FeFET Memory Based PIM Accelerator for Graph Convolutional Networks	49
<i>Hongtao Zhong, Yu Zhu, Longfei Luo, Taixin Li, Chen Wang, Yixin Xu, Tianyi Wang, Yao Yu, Vijaykrishnan Narayanan, Yongpan Liu, Liang Shi, Huazhong Yang and Xueqing Li</i>	
Design Exploration of Dynamic Multi-Level Ternary Content-Addressable Memory Using Nanoelectromechanical Relays .....	55
<i>Taixin Li, Hongtao Zhong, Sumitha George, Vijaykrishnan Narayanan, Liang Shi, Huazhong Yang and Xueqing Li</i>	
iTPM: Exploring PUF-based Keyless TPM for Security-by-Design of Smart Electronics...	61
<i>Venkata Karthik Vishnu Vardhan Bathalapalli, Saraju Mohanty, Elias Kougianos, Vasanth Iyer and Bibhudutta Rout</i>	

Fortified-Edge 2.0: Machine Learning based Monitoring and Authentication of PUF-Integrated Secure Edge Data Center .....	67
<i>Seema Aarella, Saraju Mohanty, Elias Kougianos and Deepak Puthal</i>	
IoMT Synthetic Cardiac Arrest Dataset for eHealth with AI-based Validation .....	73
<i>Joy Dutta and Deepak Puthal</i>	
Revolutionizing Cyber Security: Exploring the Synergy of Machine Learning and Logical Reasoning for Cyber Threats and Mitigation .....	79
<i>Deepak Puthal, Saraju Mohanty, Amit Kumar Mishra, Chan Yeob Yeun and Ernesto Damiani</i>	
Formal Temporal Characterization of Register Vulnerability in Digital Circuits .....	85
<i>Damiano Zuccala, Katell Morin-Allory, Jean-Marc Daveau and Philippe Roche</i>	
Harnessing the Effects of Process Variability to Mitigate Aging in Cloud Servers.....	91
<i>Arthur Lorenzon, Guilherme Korol, Marcelo Brandalero and Antonio Carlos Schneider Beck Filho</i>	
Evaluating an XOR-based Hybrid Fault Tolerance Technique to Detect Faults in GPU Pipelines.....	97
<i>Giani Augusto Braga, Jose Rodrigo Azambuja and Marcio M. Goncalves</i>	
Modeling and Analysis of Switched-Capacitor Converters as a Multi-port Network for Covert Communication.....	103
<i>Yerzhan Mustafa and Selcuk Kose</i>	
Using Lyapunov Exponents and Entropy to Estimate Sensitivity to Process Variability ...	109
<i>Elias de Almeida Ramos and Ricardo Reis</i>	
Dynamic Offloading Decisions for Improved Performance and Energy Efficiency in Heterogeneous IoT-Edge-Cloud Continuum.....	115
<i>Julio Costella Vicenzi, Guilherme Korol, Michael Guilherme Jordan, Wagner Ourique de Moraes, Hazem Ali, Edison Pignaton de Freitas, Mateus Beck Rutzig and Antonio Carlos Schneider Beck Filho</i>	
Resource Provisioning for CPU-FPGA Environments with Adaptive HLS-Versioning and DVFS .....	121
<i>Michael Jordan, Guilherme Korol, Tiago Knorst, Mateus Rutzig and Antonio Carlos Schneider Beck Filho</i>	
Design-Space Exploration of Multiplier Approximation in CNNs.....	127
<i>Raghava S N, Prashanth H C, Bindu G Gowda, Pratyush Nandi and Madhav Rao</i>	
Machine Learning and Polynomial Chaos models for Accurate Prediction of SET Pulse Current .....	133
<i>Vishu Saxena, Yash Jain and Sparsh Mittal</i>	
A 3 TOPS/W RISC-V Parallel Cluster for Inference of Fine-Grain Mixed-Precision Quantized Neural Networks .....	139
<i>Alessandro Nadalini, Georg Rutishauser, Alessio Burrello, Nazareno Bruschi, Angelo Garofalo, Luca Benini, Francesco Conti and Davide Rossi</i>	

CWAHA: Cluster-Wise Approximation for Hardware implementation of Arithmetic functions.....	145
<i>Omkar Ratnaparkhi and Madhav Rao</i>	
Column-Weighted Probabilistic GDBF Decoder for Irregular LDPC Codes.....	151
<i>Changfu He, Keyue Deng, Suwen Song and Zhongfeng Wang</i>	
Reverse Engineering of RTL Controllers from Look-Up Table Netlists.....	157
<i>Sundarakumar Muthukumaran, Aparajithan Nathamuni Venkatesan, Kishore Pula, Ram Venkat Narayanan, Ranga Vemuri and John Emmert</i>	
Performance Optimized Clock Tree Embedding for Auto-Generated FPGAs.....	163
<i>Grant Brown, Ganesh Gore and Pierre-Emmanuel Gaillardon</i>	
An FPGA-Based Reconfigurable CNN Training Accelerator Using Decomposable Winograd.....	169
<i>Hui Wang, Jinming Lu, Jun Lin and Zhongfeng Wang</i>	
DREAM: Distributed Reinforcement Learning Enabled Adaptive Mixed-Critical NoC.....	175
<i>Nidhi Anantharajiah, Yunhe Xu, Fabian Lesniak, Tanja Harbaum and Juergen Becker</i>	
Power, Performance and Reliability Evaluation of Multi-thread Machine Learning Inference Models Executing in Multicore Edge Devices.....	181
<i>Geancarlo Abich, Anderson Ignacio da Silva, José Eduardo Thums, Rafael da Silva, Altamiro Amadeu Susin, Ricardo Reis and Luciano Ost</i>	
A Secure Design Methodology to Prevent Targeted Trojan Insertion during Fabrication...	187
<i>Arjun Suresh, Siva Nishok Dhanuskodi and Daniel Holcomb</i>	
Application Profiling Using Register-Instruction Hardware Performance Counters.....	193
<i>Anand Menon, Amisha Srivastava, Shamik Kundu and Kanad Basu</i>	
Benchmarking of SoC-level Hardware Vulnerabilities: A Complete Walkthrough.....	199
<i>Shams Tarek, Hasan Al Shaikh, Sree Ranjani Rajendran and Farimah Farahmandi</i>	
Revisiting Trojan Insertion Techniques for Post-Silicon Trojan Detection Evaluation.....	205
<i>Vedika Saravanan, Mohammad Walid Charrwi and Samah Mohamed Saeed</i>	
Design and Evaluation of M-Term Non-Homogeneous Hybrid Karatsuba Polynomial Multiplier.....	211
<i>Sanampudi Gopala Krishna Reddy, Gogireddy Ravi Kiran Reddy, Vasanthi D R and Madhav Rao</i>	
LAT-UP: Exposing Layout-Level Analog Hardware Trojans Using Contactless Optical Probing.....	217
<i>Sajjad Parvin, Mehran Goli, Thilo Krachenfels, Shahin Tajik, Jean-Pierre Seifert, Frank Sill Torres and Rolf Drechsler</i>	
Machine Learning Techniques for Pre-CTS Identification of Timing Critical Flip-Flops....	223
<i>Chunkai Fu, Ben Trombley, Hua Xiang, Gi-Joon Nam and Jiang Hu</i>	
LEX - A Cell Switching Arcs Extractor: A Simple SPICE-Input Interface for Electrical Characterization.....	229
<i>Rodrigo Wuerdig, Vitor Maciel, Ricardo Reis and Sergio Bampi</i>	

3D-TTP: Efficient Transient Temperature-Aware Power Budgeting for 3D-Stacked Processor-Memory Systems .....	235
<i>Sobhan Niknam, Yixian Shen, Anuj Pathania and Andy Pimentel</i>	
Compact Model Parameter Extraction using Bayesian Machine Learning .....	241
<i>Sachin Bhat, Sourabh Kulkarni and Csaba Andras Moritz</i>	
A MCU-robust Interleaved Data/Detection SRAM for Space Environments .....	247
<i>Leonardo H. Brendler, Hervé Lapuyade, Yann Deval, Ricardo Reis and François Rivet</i>	
Efficient Accelerator Design in High-Level Synthesis Using Approximate Logic Components .....	253
<i>Tiago Almeida and Lucas Wanner</i>	
FastNTT: Design and Evaluation of Modular-Reduction based Fast NTT Design on FPGA	259
<i>Harshita Gupta, Asmita Zjiggasu, Mayank Kabra and Madhav Rao</i>	
CellFlow: Automated Standard Cell Design Flow .....	265
<i>Prashanth H C, Prashanth Jonna and Madhav Rao</i>	
Design Space Exploration for CNN Offloading to FPGAs at the Edge.....	270
<i>Guilherme Korol, Michael Jordan, Mateus Rutzig, Jeronimo Castrillon and Antonio Carlos Schneider Beck Filho</i>	
Efficient Hardware Design for the VVC Affine Motion Compensation Exploiting Multiple Constant Multiplication.....	276
<i>Marcello Munoz, Denis Maass, Murilo Perleberg, Luciano Agostini and Marcelo Porto</i>	
X4-RARE: Revisiting the X4CP32 Coarse-Grained Reconfigurable Architecture Model ...	282
<i>Ivan Silva and Francisco Junior</i>	
L-BANCS: A Multi-Phase Tile Design for Nanomagnetic Logic .....	288
<i>Ruan Formigoni, Ricardo Ferreira, Omar Paranaiba and José Augusto Nacif</i>	
Grep: Performance Enhancement in MultiCore Processors using an Adaptive Graph Prefetcher.....	294
<i>Indranee Kashyap, Dipika Deb and Nityananda Sarma</i>	
An Investigation into the Security of Register Allocation with Spilling and Splitting .....	300
<i>Priyanka Panigrahi and Chandan Karfa</i>	
Exploiting Routing Asymmetry for APUF Implementation in FPGA: A Proof of Concept	306
<i>Trishna Rajkumar</i>	