2023 IEEE International Test Conference India (ITC India 2023)

Bangalore, India 23-25 July 2023



IEEE Catalog Number: CFP23N34-POD ISBN:

979-8-3503-1215-7

Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP23N34-POD

 ISBN (Print-On-Demand):
 979-8-3503-1215-7

 ISBN (Online):
 979-8-3503-1214-0

ISSN: 2833-8383

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

E-mail: curran@proceedings.com Web: www.proceedings.com

(845) 758-2633

proceedings

Fax:

ITC India 2023 Table of Contents

Table of Contents

Addressing physically aware diagnosis challenges in hierarchical core based designs Bharath Nandakumar, Sameer Chillarige, Robert C Redburn, Jeff Zimmerman and Nicholai L'Esperance	1
Machine Learning Based MBIST Area Estimation	9
Hidden in Plain Sight: A Detailed Investigation of Selectively Increasing Local Density to Camouflage and Robustify Against Optical Probing Attacks	14
An SoC based Cost Effective Static Linearity Test Scheme for ADCs	20
Unified Analog Mixed-Signal Defect Simulation and Applications	25
Scalable and Comprehensive approach for Concurrency Validation to improve Platform Stability	31
Hardware Simulator : Virtual Testing and Non-Product Failure Isolation	36
Parallel Functional Test : A case study to reduce test cost in large SOCs	41
MBIST-HSIO Concurrent Testing Strategies and Test Challenges	47
Design of a Fault-Tolerant Pseudo-3D Routing	53
A formal approach to improve connectivity coverage in DFD, DFT, DFM, and DFX domain	59
Power Domain Aware DFT Implementation	64
A novel approach to identifying scan issues during RTL validation	72

ITC India 2023 Table of Contents

Prevention of High Current Events during Hot Testing at Turbo Frequency	5
Analysis of Non-idealities in On-chip Loopback Testing of Data Converters 7 Tamajeet Mandal, Aswin R and Rubin Parekhji	9
MBIST Area & Test Time Optimization Using Machine Learning Techniques 8 Darakshan Jamal and Ratheesh Thekke Veetil	5
Bridging Repairability Gaps in Shared Bus Architecture with Shared Physical Memory Implementation	4
PROTECTS: Secure Provisioning of System-on-Chip Assets in Untrusted Testing Facility 10 Patanjali Slpsk, Jonathan Cruz, Sandip Ray and Swarup Bhunia	0
Invisible Scan for Protecting against Scan-based Attacks: You Can't Attack What You Can't See	6
A novel test data compaction method with improved debug capabilities of the signatures . 11 $\it Jaidev~Shenoy,~Kelly~Ockunzzi~and~Dr.~Virendra~Singh$	2