2023 IEEE Symposium on VLSI Technology and Circuits
(VLSI Technology and Circuits 2023)

Kyoto, Japan
11-16 June 2023

IEEE Catalog Number: CFP23VTS-POD
ISBN: 979-8-3503-4669-5

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP23VTS-POD
ISBN (Print-On-Demand):	979-8-3503-4669-5
ISBN (Online):	978-4-86348-806-9
ISSN:	0743-1562

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

A Wireless Sensor-Brain Interface System for Tracking and Guiding Animal Behaviors Through Goal-Directed Closed-Loop Neuromodulation 1
Yi Zhu, Yuhan Hou, Jack Ji, Aaron Zhou, Andrew G. Richardson, Xilin Liu

A Wireless Neural Stimulator IC for Cortical Visual Prosthesis..... 3
Jungho Lee, Joseph Letner, Jongyup Lim, Yi Sun, Seokhyeon Jeong, Yejoong Kim, Beomseo Koo, Gabriele Atzeni, Jiawei Liao, Julianna Richie, Elena Della Valle, Paras Patel, Taekwang Jang, Cynthia Chestek, Jamie Phillips, James Weiland, Dennis Sylvester, Hun-Seok Kim, David Blaauw

A 1024-Channel 268 nW/Pixel 36x36 μm^2/Ch Data-Compressive Neural Recording IC for High-Bandwidth Brain-Computer Interfaces..... 5
Moonhyung Jang, Wei-Han Yu, Changuk Lee, Maddy Hays, Pingyu Wang, Nick Vitale, Pulkit Tandon, Pumiao Yan, Pui-In Mak, Youngcheol Chae, E. J. Chichilnisky, Boris Murmann, Dante G. Muratore

A 1,024-Channel, 64-Interconnect, Capacitive Neural Interface Using a Cross-Coupled Microelectrode Array and 2-Dimensional Code-Division Multiplexing 7
Woojun Choi, Yiyang Chen, Donghwan Kim, Sean Weaver, Tilman Schlotter, Can Livanelioglu, Jiawei Liao, Rosario Incandela, Parham Davami, Gabriele Atzeni, Sina Arjmandpour, Seong-Hwan Cho, Taekwang Jang

A Wireless, Mechanically Flexible, 25µm-Thick, 65,536-Channel Subdural Surface Recording and Stimulating Microelectrode Array with Integrated Antennas 9
Nanyu Zeng, Taesung Jung, Mohit Sharma, Guy Eichler, Jason Fabbri, R. James Cotton, Eleonora Spinazzi, Brett Youngerman, Luca Carloni, Kenneth L. Shepard

A 1Tb 3b/Cell 3D-Flash Memory of More than 17Gb/mm^2 Bit Density with 3.2Gbps Interface and 205MB/s Program Throughput.....11
M. Sako, T. Nakajima, F. Kono, T. Nakano, M. Fujiu, J. Musha, D. Nakamura, N. Kanagawa, Y. Shimizu, K. Yanagidaira, T. Utsumi, T. Kawano, Y. Hosomura, H. Yabe, M. Kano, H. Sugawara, A. H. Sravan, K. Hayashi, T. Kouchi, Y. Watanabe

A 14nm 128Mb Embedded MRAM Macro Achieved the Best Figure-Of-Merit with 80MHz Read Operation and 18.1Mb/mm^2 Implementation at 0.64V..... 13
Gyuseong Kang, Hyunjin Shin, Hyuntaek Jung, Sunkyu Lee, Jaeseung Choi, Sangyeop Baek, Hyunsung Jung, Daeshik Kim, Sohee Hwang, Shinhee Han, Yongsung Ji, Sei Seung Yoon

A 3.0 Gb/s/Pin 4^{th} Generation F-Chip with Toggle 5.0 Specification for 16Tb NAND Flash Memory Multi Chip Package 15
Youngmin Jo, Anil Kavala, Tongsung Kim, Byungkwan Chun, Jung-June Park, Taesung Lee, Jungmin Seo, Manjae Yang, Taehyeon Park, Hyunjin Kwon, Cheolhui Lee, Younghoon Son, Junghwan Kwak, Younggyu Lee, Hwan Seok Ku, Daehoon Na, Changyeon Yu, Jonghoon Park, Jaehwan Kim, Hyojin Kwon, Chanho Kim, Moon-Ki Jung, Chanjin Park, Donghyun Seo, Moosung Kim, Seungjae Lee, Jin-Yub Lee, Dongku Kang, Chiweon Yoon, Sunghoi Hur

A 40 nm 2 Kb MTJ-Based Non-Volatile SRAM Macro with Novel Data-Aware Store Architecture for Normally off Computing..... 17
Kenta Suzuki, Keizo Hiraga, Kazuhiro Bessho, Kimiyoshi Usami, Taku Umebayashi

3.7-GHz Multi-Bank High-Current Single-Port Cache SRAM with 0.5V-1.4V Wide Voltage Range Operation in 3nm FinFET for HPC Applications 19
Yoshiaki Osada, Takaaki Nakazato, Koji Nii, Jhon-Jhy Liaw, Shien-Yang Michael Wu, Quincy Li, Hidehiro Fujiwara, Hung-Jen Liao, Tsung-Yung Jonathan Chang

A 26.4mW, 18.6MS/s Image Reconstruction Processor for IoT Compressive Sensing..... 21
Yu-Cheng Lin, Chanmin Park, Wenda Zhao, Nan Sun, Youngcheol Chae, Chia-Hsiang Yang

A 169mW Fully-Integrated Ultrasound Imaging Processor Supporting Advanced Modes for Hand-Held Devices 23
Yi-Lin Lo, Yu-Chen Lo, Chia-Hsiang Yang

A 183.4nJ/Inference 152.8µW Single-Chip Fully Synthesizable Wired-Logic DNN Processor for Always-On 35 Voice Commands Recognition Application..... 25
Atsutake Kosuge, Rei Sumikawa, Yao-Chung Hsu, Kota Shiba, Mototsugu Hamada, Tadahiro Kuroda

A 12-Nm 0.62-1.61 mW Ultra-Low Power Digital CIM-Based Deep-Learning System for End-To-End Always-On Vision 27
En-Jui Chang, Cheng-Xin Xue, Chetan Deshpande, Gajanan Jedhe, Jenwei Liang, Chih-Chung Cheng, Hung-Wei Lin, Chia-Da Lee, Sushil Kumar, Kim Soon Jway, Zijie Guo, Ritesh Garg, Allen-Cl Lu, Chien-Hung Lin, Meng-Han Hsieh, Tsung-Yao Lin, Chih-Cheng Chen

A 6.4-GS/s 1-GHz BW Continuous-Time Pipelined ADC with Time-Interleaved Sub-ADC-DAC Achieving 61.7-DB SNDR in 16-Nm FinFET 29
Rishabh Mittal, Hajime Shibata, Sharvil Patil, Erik Krommenhoek, Prawal Shrestha, Gabriele Manganaro, Anantha P. Chandrakasan, Hae-Seung Lee

A 0.024mm² 84.2dB-SNDR 1MHz-BW 3rd-Order VCO-Based CTDSM with NS-SAR Quantizer (NSQ VCO CTDSM) 31
Hsiang-Wen Chen, Seungjong Lee, Michael Flynn

A 6GHz Multi-Path Multi-Frequency Chopping CTΔΣ Modulator Achieving 122dBFS SFDR from 150kHz to 120MHz BW..... 33
Sundeep Javvaji, Muhammed Bolatkale, Shagun Bajoria, Robert Rutten, Bert Oude Essink, Koen Beijens, Kofi Makinwa, Lucien Breems

A 4.4 GS/s 220 MHz ΣΔ ADC with a Linearized Back-Gate Controlled GmC Filter..... 35
Julius Edler, Marcel Runge, Sebastian Linnhoff, Friedel Gerfers

A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-Bit Delta-Sigma Modulator and Transformer Combined FIR FIlter 37
Yuncheng Zhang, Zheng Sun, Bangan Liu, Junjun Qiu, Dingxin Xu, Yi Zhang, Xi Fu, Dongwon You, Hongye Huang, Waleed Madany, Ashbir Aviat Fadila, Zezheng Liu, Wenqian Wang, Yuang Xiong, Atsushi Shirane, Kenichi Okada

An 8.7 mW/TX, 21 mW/RX 6-To-9GHz IEEE 802.15.4a/4z Compliant IR-UWB Transceiver with Pulse Pre-Emphasis Achieving 14mm Ranging Precision..... 39
Minyoung Song, Erwin Allebes, Chris Marshall, Anoop Narayan Bhat, Elbert Bechthum, Johan Dijkhuis, Stefano Traferro, Evgenii Tiurin, Peter Vis, Johan Van Den Heuvel, Mohieddine El Soussi, Pepijn Boer, Alireza Sheikh, Bernard Meyer, Jiang Liu, Stan Van Der Ven, Nick Winkel, Martijn Hijdra, Gururaja Kasanadi Ramachandra, Yunus Baykal, Huib Visser, Peng Zhang, Arjan Breeschoten, Yao-Hong Liu, Christian Bachmann

A 6.5nW, -73.5dBm Sensitivity, Cryptographic Wake-Up Receiver with a PUF-Based OTP and Temperature-Insensitive Code Recovery 41
Jaehan Park, Cheonhoo Jeon, Donggyu Minn, Heesung Roh, Jae-Yoon Sim

An All-Digital Outphasing Transmitter IC for Ka-Band Bit-To-RF Concurrent Multi-Beam DBF Array 43
Dong Wang, Jiazheng Zhou, Hui Xu, Ningyuan Zhang, Xiaolei Su, Zhengkun Shen, Haoyun Jiang, Fan Yang, Yixiao Wang, Junhua Liu, Huailin Liao

A 112-Gb/s 58-MW PAM4 Transmitter in 28-Nm CMOS Technology 45
Mahdi Forghani, Yu Zhao, Pawan K. Khanna, Behzad Razavi

A 256 Gbps Heterogeneously Integrated Silicon Photonic Microring-Based DWDM Receiver Suitable for In-Package Optical I/O 47
Zhe Xuan, Ganesh Balamurugan, Duanni Huang, Ranjeet Kumar, Jahnavi Sharma, Cooper Levy, Jinyong Kim, Chaoxuan Ma, Guan-Lin Su, Songtao Liu, Xinru Wu, Tolga Acikalin, Haisheng Rong, James Jaussi

A 0.32pJ/b 90Gbps PAM4 Optical Receiver Front-End with Automatic Gain Control in 12nm CMOS FinFET 49
Milad Haghi Kashani, Hossein Shakiba, Ali Sheikholeslami

A 64-Gb/s Reference-Less PAM4 CDR with Asymmetrical Linear Phase Detector Soring 231.5-fs_{rms} Clock Jitter and 0.21-PJ/bit Energy Efficiency in 40-Nm CMOS 51
Zhao Zhang, Zhaoyu Zhang, Yong Chen, Nan Qi, Jian Liu, Nanjian Wu, Liyuan Liu

A 50Gb/s DAC-Based Multicarrier Polar Transmitter in 22nm FinFET 53
Il-Min Yi, Srujan Kumar Kaile, Yuanming Zhu, Julian Camilo Gomez Diaz, Sebastian Hoyos, Samuel Palermo

Arvon: A Heterogeneous SiP Integrating a 14nm FPGA and Two 22nm 1.8TFLOPS/W DSPs with 1.7Tbps/mm^2 AIB 2.0 Interface to Provide Versatile Workload Acceleration 55
Wei Tang, Sung-Gun Cho, Tim Tri Hoang, Jacob Botimer, Wei Qiang Zhu, Ching-Chi Chang, Cheng-Hsun Lu, Junkang Zhu, Yaoyu Tao, Tianyu Wei, Naomi Kavi Motwani, Mani Yalamanchi, Ramya Yarlagadda, Sirisha Kale, Mark Flanigan, Allen Chan, Thungoc Tran, Sergey Shumarayev, Zhengya Zhang

A 4.8mW, 800Mbps Hybrid Crypto SoC for Post-Quantum Secure Neural Interfacing 57
Liang-Hsin Lin, Zih-Sing Fu, Po-Shao Chen, Bo-Yin Yang, Chia-Hsiang Yang

A Bit-Serial Computing Accelerator for Solving Coupled Partial Differential Equations 59
Junjie Mu, Chengshuo Yu, Tony Tae-Hyoung Kim, Bongjin Kim

A 2.35 Gb/s/mm^2 (7440, 6696) NB-LDPC Decoder Over GF(32) Using Memory-Reduced Column-Wise Trellis Min-Max Algorithm in 28nm CMOS Technology 61
Jeongwon Choe, Youngjoo Lee

A 65nm 60mW Dual-Loop Adaptive Digital Beamformer with Optimized Sidelobe Cancellation and On-Chip DOA Estimation for mm-Wave Applications 63
Sigang Ryu, Adou Sangbone Assoa, Shota Konno, Arijit Raychowdhury

Wireless Body-Area Network Transceiver ICs with Concurrent Body-Coupled Powering and Communication Using Single Electrode 65
Jiamin Li, Yilong Dong, Longyang Lin, Joanne Si Ying Tan, Fong Jia Yi, Jerald Yoo

A Fingertip-Mimicking 12×16 200µm-Resolution E-Skin Taxel Readout Chip with per-Taxel Spiking Readout and Embedded Receptive Field Processing 67
Mark Daniel Alea, Ali Safa, Flavio Giacomozzi, Andrea Adami, Inci Rüya Temel, Leandro Lorenzelli, Georges Gielen

A 110dB-TCMRR TDM-Based 8-Channel Noncontact ECG Recording IC with Suppression of Motion-Induced Coupling in <0.3s and CMI Cancellation Up to $22V_{PP}$ 69
Kyu-Jin Choi, Seungnam Choi, Jae-Yoon Sim

A Pitch-Matched Transceiver ASIC for 3D Ultrasonography with Micro-Beamforming ADCs Based on Passive Boxcar Integration and a Multi-Level Datalink 71
P. Guo, Z. Y. Chang, E. Noothout, H. J. Vos, J. G. Bosch, N. De Jong, M. D. Verweij, M. A. P. Pertijs

A CMOS/Microfluidics Point-Of-Care SoC Employing Square-Wave Voltcoulometry for Biosensing with Aptamers and CRISPR-Cas12a Enzymes 73
Yan-Ting Hsiao, Shu-Yan Chuang, Hung-Yu Hou, Yun-Chun Su, Hsiu-Cheng Yeh, Hsin-Tzu Song, Yun-Jui Chang, Wei-Yang Weng, Ya-Chen Tsai, Pin-Yu Lin, Sih-Ying Chen, Yen-Ju Lin, Mei-Wei Lin, Jun-Chau Chien

A 3nm 256Mb SRAM in FinFET Technology with New Array Banking Architecture and Write-Assist Circuitry Scheme for High-Density and Low-V_{MIN} Applications 75
Jonathan Chang, Yen-Huei Chen, Gary Chan, Kuo-Cheng Lin, Po-Sheng Wang, Yangsyu Lin, Sevic Chen, Peijiun Lin, Ching-Wei Wu, Chih-Yu Lin, Yi-Hsin Nien, Hidehiro Fujiwara, Atul Katoch, Robin Lee, Hung-Jen Liao, Jhon-Jhy Liaw, Shien-Yang Michael Wu, Quincy Li

A 1.9GHz 0.57V Vmin 576Kb Embedded Product-Ready L2 Cache in 5nm FinFET Technology 77
N. Jungmann, R. Joshi, E. Kachir, K. Shimanovich, B. He, T. Cohen, T. Miller, D. Leu, D. Kannambadi, I. Wagner, K. Reyer, H. Konen, M. Suleiman, V. Sindhe, Y. Freiman

A 4.0GHz UHS Pseudo Two-Port SRAM with BL Charge Time Reduction and Flying Word-Line for HPC Applications in 4nm FinFET Technology 79
Jeongkyun Kim, Byungho Yook, Taemin Choi, Kyuwon Choi, Chanho Lee, Yunrong Li, Youngo Lee, Seok Yun, Changhoon Do, Hoyoung Tang, Inhak Lee, Dongwook Seo, Sangyeop Baeck

A 4.24GHz 128X256 SRAM Operating Double Pump Read Write Same Cycle in 5nm Technology 81
Nick Zhang, Young Suk Kim, Peter Hsu, Samsoo Kim, Derek Tao, Hung-Jen Liao, P. W. Wang, Geoffrey Yeap, Quincy Li, Tsung-Yung Jonathan Chang

A 3-Nm 27.6-Mbit/mm^2 Self-Timed SRAM Enabling 0.48 - 1.2 V Wide Operating Range with Far-End Pre-Charge and Weak-Bit Tracking 83
Yumito Aoyagi, Makoto Yabuuchi, Tomotaka Tanaka, Yuichiro Ishii, Yoshiaki Osada, Takaaki Nakazato, Koji Nii, Isabel Wang, Yu-Hao Hsu, Hong-Chen Cheng, Hung-Jen Liao, Tsung-Yung Jonathan Chang

A 2.38 MCells/mm^2 9.81 -350 TOPS/W RRAM Compute-In-Memory Macro in 40nm CMOS with Hybrid Offset/I_{OFF} Cancellation and $I_{CELL}R_{BLSL}$ Drop Mitigation 85
Samuel D. Spetalnick, Muya Chang, Shota Konno, Brian Crafton, Ashwin S. Lele, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Arijit Raychowdhury

A 28nm Nonvolatile AI Edge Processor Using 4Mb Analog-Based Near-Memory-Compute ReRAM with 27.2 TOPS/W for Tiny AI Edge Devices 87
Tai-Hao Wen, Je-Min Hung, Hung-Hsi Hsu, Yuan Wu, Fu-Chun Chang, Chung-Yuan Li, Chih-Han Chien, Chin-I Su, Win-San Khwa, Jui-Jen Wu, Chung-Chuan Lo, Ren-Shuo Liu, Chih-Cheng Hsieh, Kea-Tiong Tang, Mon-Shu Ho, Yu-Der Chih, Tsung-Yung Jonathan Chang, Meng-Fan Chang

Scaling-CIM: An eDRAM-Based In-Memory-Computing Accelerator with Dynamic-Scaling ADC for SQNR-Boosting and Layer-Wise Adaptive Bit-Truncation 89
Sangiin Kim, Soyeon Um, Wooyoung Jo, Jingu Lee, Sangwoo Ha, Zhiyong Li, Hoi-Jun Yoo

A 12nm 137 TOPS/W Digital Compute-In-Memory Using Foundry 8T SRAM Bitcell Supporting 16 Kernel Weight Sets for AI Edge Applications 91
Gajanan Jedhe, Chetan Deshpande, Sushil Kumar, Cheng-Xin Xue, Zijie Guo, Ritesh Garg, Kim Soon Jway, En-Jui Chang, Jenwei Liang, Zhe Wan, Zhenhao Pan

SP-PIM: A 22.41TFLOPS/W, 8.81Epochs/Sec Super-Pipelined Processing-In-Memory Accelerator with Local Error Prediction for On-Device Learning 93
Jung-Hoon Kim, Jaehoon Heo, Wontak Han, Jaeuk Kim, Joo-Young Kim

A 0.05-To-3.1A 585mA/mm^3 97.3%-Efficiency Outphase Switched-Capacitor Hybrid Buck Converter with Relieved Capacitor Inrush Current and C_{OUT}-Free Operation 95
Xiongjie Zhang, Qiaobo Ma, Anyang Zhao, Yang Jiang, Man-Kay Law, Pui-In Mak, Rui Martins

96.48% Peak-Efficiency Continuous-Current Step-Up Battery Charger (CC-SUBC) with Dual Energy-Harvesting Sources for Automotive Application 97
Hyo-Jin Park, Joo-Mi Cho, Hyeon-Ji Choi, Chan-Ho Lee, Sung-Wan Hong

A 19.8W/29.6W Hybrid Step-Up/Down DC-DC Converter with 97.2% Peak Efficiency for 1-Cell/2-Cell Battery Charger Applications 99
Seongil Yeo, Uyong Hyeon, Mingyeong Kim, Jusung Kim, Kunhee Cho

A 4.1W/mm² Peak Power Density and 77% Peak Efficiency Fully Integrated DC-DC Converter Based on Electromagnetically Coupled Class-D LC Oscillators and a Resonant LC Flying Impedance in 22nm FDSOI CMOS 101
Alessandro Novello, Gabriele Atzeni, Tim Keller, Taekwang Jang

A Fully Synthesizable 100Mbps Edge-Chasing True Random Number Generator 103
Yan He, Kaiyuan Yang

218Kauth/s, 3nJ/Auth SCA/ML-Resistant Privacy-Preserving Mutual Authentication Accelerator with a Crypto-Double-Coupled PUF in 4nm Class CMOS 105
Sachin Taneja, Vikram Suresh, Raghavan Kumar, Vivek De, Sanu Mathew

ECC-Less Multi-Level SRAM Physically Unclonable Function and 127% PUF-To-Memory Capacity Ratio with No Bitcell Modification in 28nm 107
Joydeep Basu, Sachin Taneja, Viveka Konandur Rajanna, Tianqi Wang, Massimo Alioto

A Static Contention-Free Dual-Edge-Triggered Flip-Flop with Redundant Internal Node Transition Elimination for Ultra-Low-Power Applications 109
Sekeon Kim, Keonhee Cho, Kyeongrim Baek, Hyunjun Kim, Younmee Bae, Mijung Kim, Dongwook Seo, Sangyeop Baeck, Sungjae Lee, Seong-Ook Jung

A Sub-THz Full-Duplex Phased-Array Transceiver with Self-Interference Cancellation and LO Feedthrough Suppression 111
Chun Wang, Ibrahim Abdo, Chenxin Liu, Carrel Da Gomez, Hans Herdian, Wenqian Wang, Xi Fu, Dongwon You, Abanob Shehata, Sunghwan Park, Yun Wang, Jian Pang, Hiroyuki Sakai, Atsushi Shirane, Kenichi Okada

An 11.4-To-16.4GHz FMCW Digital PLL with Cycle-Slipping Compensation and Back-Tracking DPD Achieving 0.034% RMS Frequency Error Under 3.4-GHz Chirp Bandwidth and 960-MHz/μs Chirp Slope....113
Angxiao Yan, Wei Deng, Haikun Jia, Shiyan Sun, Chao Tang, Bufan Zhu, Yu Fu, Hongzhuo Liu, Baoyong Chi

An 18.8-To-23.3 GHz ADPLL Based on Charge-Steering-Sampling Technique Achieving 75.9 Fs RMS Jitter and –252 dB FoM....115
Weichen Tao, Weichen Zhao, Robert Bogdan Staszewski, Fujiang Lin, Yizhe Hu

A 24-30 GHz Cascaded QPLL Achieving 56.8-Fs RMS Jitter and −248.6-DB FoM_{jitter}....117
Li Wang, Zilu Liu, C. Patrick Yue

A 2GS/s 11b 8x Interleaved ADC with 9.2 ENOB and 69.9dB SFDR in 28nm CMOS 119
Luca Ricci, Lorenzo Scaletti, Gabriele Bè, Michele Rocco, Luca Bertulessi, Salvatore Levantino, Andrea Lacaita, Carlo Samori, Andrea Bonfanti

A 79.5dB-SNDR Pipelined-SAR ADC with a Linearity-Shifting 32× Dynamic Amplifier and Mounted-Over-Die Bypass Capacitors.... 121
Minglei Zhang, Yuefeng Cao, Yan Zhu, Chi-Hang Chan, R. P. Martins

A 150-MS/s Fully Dynamic SAR-Assisted Pipeline ADC Using a Floating Ring Amplifier and Gain-Enhancing Miller Negative-C.... 123
Seungheun Song, Taewook Kang, Seungjong Lee, Michael P. Flynn

A 0.75V 0.016mm^2 12ENOB 7nm CMOS Cyclic ADC with 1.5bit Passive Amplification Stage and Dynamic Capacitance Scaling.... 125
Takashi Oshima, Keisuke Yamamoto, Goichi Ono

An Indirect Time-Of-Flight CMOS Image Sensor Achieving Sub-Ms Motion Lagging and 60fps Depth Image from On-Chip ISP.... 127
Jiheon Park, Daeyun Kim, Hoyong Lee, Seung-Chul Shin, Myoungoh Ki, Bumsik Chung, Myunghan Bae, Myeonggyun Kye, Jonghan Ahn, Inho Song, Sunhwa Lee, Jaeil An, Il-Pyeong Hwang, Taemin An, Young-Gu Jin, Youngchan Kim, Youngsun Oh, Juhyun Ko, Haechang Lee, Joonseo Yim

A 3.36 μm-Pitch SPAD Photon-Counting Image Sensor Using Clustered Multi-Cycle Clocked Recharging Technique with Intermediate Most-Significant-Bit Readout.... 129
T. Takatsuka, J. Ogi, Y. Ikeda, K. Hizu, Y. Inaoka, S. Sakama, I. Watanabe, T. Ishikawa, S. Shimada, J. Suzuki, H. Maeda, K. Toshima, Y. Nonaka, A. Yamamura, H. Ozawa, F. Koga, Y. Oike

A Monolithic Amorphous-Selenium/CMOS Small-Pixel-Effect-Enhanced X-Ray-Energy-Discriminating Quantum-Counting Pixel for Biomedical Imaging.... 131
Reza Mohammadi, Peter M. Levine, Karim S. Karim

A −20°C~+107°C 52mk-NETD Reference-Cell-Free 15-Bits ROIC for 80×60 Micro-Bolometer Thermal Imager.... 133
Hsin Yu, John Carl Joel Salao Marquez, Chih-Cheng Hsieh

A 28 nm 66.8 TOPS/W Sparsity-Aware Dynamic-Precision Deep-Learning Processor 135
Hangyeol Mun, Hyunwoo Son, Seunghyun Moon, Jaehyun Park, Byungjun Kim, Jae-Yoon Sim

ANP-G: A 28nm 1.04pJ/SOP Sub-mm^2 Spiking and Back-Propagation Hybrid Neural Network Asynchronous Olfactory Processor Enabling Few-Shot Class-Incremental On-Chip Learning 137
Dexuan Huo, Jilin Zhang, Xinyu Dai, Jian Zhang, Chunqi Qian, Kea-Tiong Tang, Hong Chen

A Switched-Capacitor Integer Compute Unit with Decoupled Storage and Arithmetic for Cloud AI Inference in 5nm CMOS 139
Ankur Agrawal, Monodeep Kar, Kyu-Hyoun Kim, Sergey Rylov, Jinwook Jung, Seiji Munetoh, Kohji Ho-Sokawa, Xin Zhang, Bahman Hekmatshoartabari, Fabio Carta, Martin Cochet, Robert Casatuta, Mingu Kang, Sunil Shukla, Kailash Gopalakrishnan, Leland Chang

Pianissimo: A Sub-MW Class DNN Accelerator with Progressive Bit-By-Bit Datapath Architecture for Adaptive Inference at Edge 141
Junnosuke Suzuki, Jaehoon Yu, Mari Yasunaga, Ángel López García-Arias, Yasuyuki Okoshi, Shungo Kumazawa, Kota Ando, Kazushi Kawamura, Thiem Van Chu, Masato Motomura

A 28nm 77.35TOPS/W Similar Vectors Traceable Transformer Processor with Principal-Component-Prior Speculating and Dynamic Bit-Wise Stationary Computing 143
Yang Wang, Yubin Qin, Dazheng Deng, Xiaolong Yang, Zhiren Zhao, Ruiqi Guo, Zhiheng Yue, Leibo Liu, Shaojun Wei, Yang Hu, Shouyi Yin

A Fully Integrated 230 V_{RMS}-To-12 V_{DC} AC-DC Converter Achieving 9 mW/mm^2 145
Tuur Van Daele, Filip Tavernier

5G NR RF PA Supply Modulator Supporting 179ns 0.5-To-5.5V Symbol Power Tracking and Envelope Tracking 147
Jun-Suk Bang, Dongsu Kim, Younghwan Choo, Ik-Hwan Kim, Seungchan Park, Jeongkwang Lee, Sang-Han Lee, Young-Ho Jung, Jae-Young Ko, Sungyoub Jung, Jaeyeol Han, Woosik Kim, Ji-Seon Paek, Jongwoo Lee

A 93.5%-Efficiency 13.56-MHz-Bandwidth Optimal On/Off Tracking Active Rectifier with Fully Digital Feedback-Based Delay Control for Adaptive Efficiency Compensation 149
Jisan Ahn, Hyun-Su Lee, Kyeongho Eom, Woojoong Jung, Hyung-Min Lee

A 0.22mm^2 Per Channel Data Link for Reinforced Isolation with >25kVpk Surge Tolerance and >295kV/µs Common Mode Transient Immunity 151
Dongwan Ha, Ruida Yun, Kevin Wrenner

A 3-320 fJ/Conv.step Continuous Time Level Crossing ADC with Dynamic Self-Biasing Comparators Achieving 61.4 dB-SNDR 153
Martijn Timmermans, Marco Fattori, Pieter Harpe, Yao-Hong Liu, Eugenio Cantatore

A 24-OSR to Simplify Anti-Aliasing Filter 2MHz-BW 83dB-DR 3rd-Order DT-DSM Using FIA-Based Integrator and Noise-Shaping SAR Combined Digital Noise-Coupling Quantizer 155
Mitsuya Fukazawa, Tetsuo Matsui

A 2.5mW 12MHz-BW 69dB SNDR Passive Bandpass ΔΣ ADC with Highpass Noise-Shaping SAR Quantizers 157
Sein Oh, Seunga Park, Yoontae Jung, Jimin Koo, Donghee Cho, Sohmyung Ha, Minkyu Je

A 187dB FoM$_S$ 46fJ/Conv. 2nd-Order Highpass Δ∑ Capacitance-To-Digital Converter 159
Yoontae Jung, Sein Oh, Jimin Koo, Seunga Park, Ji-Hoon Suh, Donghee Cho, Sohmyung Ha, Minkyu Je

A Reconfigurable Analog FIR Filter Achieving −70dB Rejection with Sharp Transition for Narrowband Receivers 161
Chien-Wei Tseng, Zhen Feng, Zichen Fan, Hyochan An, Yunfan Wang, Hun-Seok Kim, David Blaauw

An Energy-Efficient Impedance-Boosted Discrete-Time Amplifier Achieving 0.34 Noise Efficiency Factor and 389 MΩ Input Impedance 163
Gabriele Atzeni, Can Livanelioglu, Lavinia Recchioni, Sina Arjmandpour, Taekwang Jang

A 1V 20.7µW Four-Stage Amplifier Capable of Driving a 4-To-12nF Capacitive Load with >1.07MHz GBW with an Improved Active Zero 165
Chan-Ho Lee, Hyo-Jin Park, Joo-Mi Cho, Hyeon-Ji Choi, Young-Jun Jeon, Sung-Wan Hong

A Class-D Piezoelectric Speaker Driver Using a Quadrature Feedback Chopping Scheme Achieving 29dB Large-Signal THD+N Improvement 167
Shoubhik Karmakar, Huajun Zhang, Marco Berkhout, Qinwen Fan

A Compact 0.9uW Direct-Conversion Frequency Analyzer for Speech Recognition with Wide-Range Q-Controlable Bandpass Rectifier 169
Shiro Dosho, Ludovico Minati, Kazuki Maari, Hiroyuki Ito

A Mobile OLED Source-Driver IC Featuring Ultra-Compact 3-Stage-Cascaded 10-Bit DAC and 42V/µs-Slew-Rate True-DC-Interpolative Super-OTA Buffer 171
Seunghwa Shin, Gyeong-Gu Kang, Gyu-Wan Lim, Hyun-Sik Kim

A 16-Channel Active-Matrix Mini-LED Driver with an USI-B for EMI Noise Reduction 173
Y. Kwon, Y. Kwak, Y. Choi, K. Kim, S. Kim, W. Jang, J. Park, K. Ryu, S. Yoo, H. W. Lim, J. Y. Lee

Two-Dimensionally Arranged Display Drivers Achieved by OS/Si Structure 175
Yusuke Komura, Shoki Miyata, Yuki Okamoto, Yuki Tamatsukuri, Hiroki Inoue, Toshihiko Saito, Munehiro Kozuma, Hidetomo Kobayashi, Tatsuya Onuki, Yuichi Yanagisawa, Toshihiko Takeuchi, Yutaka Okazaki, Hitoshi Kunitake, Daiki Nakamura, Takaaki Nagata, Yasumasa Yamane, Makoto Ikeda, Shih-Ci Yen, Chuan-Hua Chang, Wen-Hsiang Hsieh, Hiroshi Yoshida, Min-Cheng Chen, Ming-Han Liao, Shou-Zen Chang, Shunpei Yamazaki

A 2048-Channel, 125µW/ch DAC Controlling a 9,216-Element Optical Phased Array Coherent Solid-State LiDAR 177
Benjamin R. Moss, Christopher V. Poulton, Matthew J. Byrd, Peter Russo, Oleg Shatrovoy, David Paquette, Andrew Reardon, Michael R. Watts

Super-Cutoff Analog Building Blocks for pW/Stage Operation and Demonstration of 78-PW Battery-Less Light-Harvested Wake-Up Receiver Down to Moonlight 179
Joydeep Basu, Luigi Fassio, Karim Ali, Massimo Alioto

A General-Purpose Compute-In-Memory Processor Combining CPU and Deep Learning with Elevated CPU Efficiency and Enhanced Data Locality 181
Yuhao Ju, Yijie Wei, Xi Chen, Jie Gu

A 709.3 TOPS/W Event-Driven Smart Vision SoC with High-Linearity and Reconfigurable MRAM PIM 183
Wenao Xie, Haoyang Sang, Beomseok Kwon, Dongseok Im, Sangjin Kim, Sangyeob Kim, Hoi-Jun Yoo

A 5.6-89.9TOPS/W Heterogeneous Computing-In-Memory SoC with High-Utilization Producer-Consumer Architecture and High-Frequency Read-Free CIM Macro 185
Jinshan Yue, Mingtao Zhan, Zi Wang, Yifan He, Yaolei Li, Songming Yu, Wenyu Sun, Lu Jie, Chunmeng Dou, Xueqing Li, Nan Sun, Huazhong Yang, Ming Liu, Yongpan Liu

GPPU: A 330.4-µJ/ Task Neural Path Planning Processor with Hybrid GNN Acceleration for Autonomous 3D Navigation 187
Seokchan Song, Donghyeon Han, Sangjin Kim, Sangyeob Kim, Gwangtae Park, Hoi-Jun Yoo

NeRPIM: A 4.2 mJ/Frame Neural Rendering Processing-In-Memory Processor with Space Encoding Block-Wise Mapping for Mobile Devices 189
Wooyoung Jo, Sangjin Kim, Juhyoung Lee, Donghyeon Han, Sangyeob Kim, Seungyoon Choi, Hoi-Jun Yoo

A 90 μW at 1 Fps and 1.33 mW at 30 Fps 120 dB Intra-Scene Dynamic Range 640 × 480 Stacked Image Sensor for Autonomous Vision Systems 191
P.-F. Rüedi, R. Quaglia, H.-R. Graf

A 320 X 320 1/5" BSI-CMOS Stacked Event Sensor for Low-Power Vision Applications 193
Guillaume Schon, Denis Bourke, Pierre-Antoine Doisneau, Thomas Finateu, Adrien Gonzalez, Naoyuki Hanajima, Tahar Hitana, Lucas Janse Van Vuuren, Moataz Kadry, Charles Laurent, Florian Le Goff, Daniel Matolin, Adel Mezaour, Benoît Michel, Thulaxan Naguleswaran, Tjaart Opperman, Patrice Perrin, Etienne Reynaud, Farzaneh Shahrokhi, Hiba Tahachouite, Chen Tianfan, Gerd Van Den Branden, Akli Ziram, Jean-Luc Jaffard, Christoph Posch

An 0.08 e^{-} · pJ/Step 14-Bit Gain-Adaptive Single-Slope Column ADC with Enhanced HDR Function for High-Quality Imagers 195
Luong Hung, Koji Matsuura, Hiroki Suto, Kazutoshi Kodama, Yosuke Tanaka, Toshiaki Ono, Junichiro Fujimagari, Kentaro Akiyama, Miho Akahide, Yoshiaki Inada

A 60fps9.9nJ/Frame·pixel CMOS Image Sensor with On-Chip Pixel-Wise Conversion Gain Modulation for Per-Frame Adaptive DCG-HDR Imaging 197
Yi Luo, Shahriar Mirabbasi

A Low-Voltage Area-Efficient TSV I/O for HBM with Data Rate Up to 15Gb/s Featuring Overlapped Multiplexing Driver, ISI Compensators and QEC 199
Taeryeong Kim, Ji-Young Kim, Jeonghyeok You, Hohyun Chae, Byoung Mo Moon, Kyomin Sohn, Seong-Ook Jung

A 0.190-PJ/bit 25.2-Gb/s/Wire Inverter-Based AC-Coupled Transceiver for Short-Reach Die-To-Die Interfaces in 5-nm CMOS 201
Yoshinori Nishi, John W. Poulton, Xi Chen, Sanquan Song, Brian Zimmer, Walker J. Turner, Stephen G. Tell, Nikola Nedovic, John M. Wilson, William J. Dally, C. Thomas Gray

A 5.2 Gb/s 3 mm Air-Gap 4.7 pJ/bit Capacitively-Coupled Transceiver for Giant Video Walls Enabled by a Dual-Edge Tracking Clock and Data Recovery Loop 203
Mohamed Badr Younis, Mostafa Ahmed, Tianyu Wang, Ahmed Abdelrahman, Mahmoud Khalil, Anup Jose, Pavan Kumar Hanumolu

A Sub-500fJ/bit 3D Direct Bond Silicon Photonic Transceiver in 12nm FinFET 205
Po-Hsuan Chang, Anirban Samanta, Peng Yan, Mingye Fu, Yu Zhang, Mehmet Berkay On, Ankur Kumar, Hyungryul Kang, Il-Min Yi, Dedeepya Annabattuni, David Scott, Robert Patti, Yang-Hang Fan, Yuanming Zhu, S. J. Ben Yoo, Samuel Palermo

A Wideband CMOS NMR Spectrometer for Multinuclear Molecular Fingerprinting 207
Aoyang Zhang, Daniel Krüger, Behdad Aghelnejad, Guang Yang, Henry Hinton, Yi-Qiao Song, Donhee Ham

A Highly-Digital PWM-Based Impedance Monitoring IC with 143.2dB DR and 17.7fF_{rms} Resolution 209
Hyeonho Han, Woojun Choi, Jaehyun Kim, Jaesuk Sung, Heon-Jin Choi, Youngcheol Chae

A 36nW CMOS Temperature Sensor with <0.1K Inaccuracy and Uniform Resolution.....211
Wei Wang, Liwen Jiang, Shayok Dutta, Yumin Su, Zhiyu Chen, Zhanghao Yu, Caleb Kemere, Kaiyuan Yang

38.4-PW, 0.14-mm^2 Body-Driven Temperature-To-Digital Converter and Voltage Reference with 0.6-1.6-V Unregulated Supply for Battery-Less Systems 213
Luigi Fassio, Orazio Aiello, Massimo Alioto

A 720 nW Current Sensor with 0-To-15 V Input Common-Mode Range and ±0.5% Gain Error from −40 to 85 °C 215
Roger Zamparette, Kofi Makinwa

Proactive Power Regulation with Real-Time Prediction and Fast Response Guardband for Fine-Grained Dynamic Voltage Droop Mitigation on Digital SoCs 217
Xi Chen, Jiaxiang Feng, Aly Shoukry, Xin Zhang, Raveesh Magod, Nachiket Desai, Jie Gu

A 2.6 mV/b Resolution, 1.2 GHz Throughput, All-Digital Voltage Droop Monitor Using Coupled Ring Oscillators in Intel 4 CMOS 219
C. Augustine, P. Meinerzhagen, W. Lim, A. Veerabathini, M. Bright, K. Mojjada, J. Tschanz, M. Khellah, V. De

Self-Referenced Design-Agnostic Laser Voltage Probing Attack Detection with 100% Protection Coverage, 58% Area Overhead for Automated Design 221
Hui Zhang, Longyang Lin, Qiang Fang, Udara Samurdhi Harshanga Kalingage, Massimo Alioto

Visual Content-Agnostic Novelty Detection Engine with 2.4 pJ/Pixel Energy and Two-Order of Magnitude DNN Activity Reduction in 40 nm..... 223
Animesh Gupta, Sayan Kumar, Viveka Konandur, Sachin Taneja, Massimo Alioto

Voltage Scaling-Agnostic Counteraction of Side-Channel Neural Net Reverse Engineering Via Machine Learning Compensation and Multi-Level Shuffling..... 225
Qiang Fang, Longyang Lin, Hui Zhang, Tianqi Wang, Massimo Alioto

A Reference-Sampling PLL with Low-Ripple Double-Sampling PD Achieving −80-DBc Reference Spur and −259-DB FoM with 12-PF Input Load..... 227
Zunsong Yang, Masaru Osada, Shuowei Li, Yuyang Zhu, Tetsuya Iizuka

A 2.4-To-4.2GHz 440.2fs$_{rms}$-Integrated-Jitter 4.3mW Ring-Oscillator-Based PLL Using a Switched-Capacitor-Bias-Based Sampling PD in 4nm FinFET CMOS 229
Jaehong Jung, Kyungmin Lee, Gunwoo Kong, Baekmin Lim, Seungjin Kim, Seunghyun Oh, Jongwoo Lee

A 6nW 30.8kHz Relaxation Oscillator with Sampling Bias-Free RC Circuit and Dynamic Power Scaling in a 12nm FinFET..... 231
Fan-Wei Liao, Shan-Chih Tsou, Chien-Sheng Chao

A 50µW Ring-Type Complementary Inverse-Class-D Oscillator with 191.4dBc/Hz FoM and 205.6dBc/Hz FoM$_A$ 233
Kai Xu, Bowen Yu, Jun Hu, Yubin Li, Robert Bogdan Staszewski, Hongtao Xu

A 122fs$_{rms}$-Jitter and −60dBc-Reference-Spur 12.24GHz MDLL with a 102 - Multiplication Factor Using a Power-Gating Technique..... 235
Yoonseo Cho, Jeonghyun Lee, Suneui Park, Seyeon Yoo, Jaehyouk Choi

Exploring Power Savings of Gate-All-Around Cryogenic Technology..... 237
Victor Moroz, Alexei Svizhenko, Munkang Choi, Plamen Asenov, Jaehyun Lee

Circuit Designs for Practical-Scale Fault-Tolerant Quantum Computing 239
Yasunari Suzuki, Yosuke Ueno, Wang Liao, Masamitsu Tanaka, Teruo Tanimoto

Long-Time-Constant Leaky-Integrating Oxygen-Vacancy Drift-Diffusion FET for Human-Interactive Spiking Reservoir Computing 241
Hisashi Inoue, Hiroto Tamura, Ai Kitoh, Xiangyu Chen, Zolboo Byambadorj, Takeaki Yajima, Yasushi Hotta, Tetsuya Iizuka, Gouhei Tanaka, Isao H. Inoue

Experimental Demonstration of Probabilistic-Bit (p-Bit) Utilizing Stochastic Oscillation of Threshold Switch Device 243
Seongjae Heo, Dongmin Kim, Wooseok Choi, Sanghyun Ban, Ohhyuk Kwon, Hyunsang Hwang

Accelerating Adaptive Parallel Tempering with FPGA-Based P-Bits 245
Navid Anjum Aadit, Masoud Mohseni, Kerem Y. Camsari

A Prototype 5nm Custom Sensor SoC for Augmented Reality/Virtual Reality Targeting Smartglasses with Embedded Computer Vision, Audio, Security and ML 247
Karl Kaiser, Dinesh Patil, Edith Beigne

A Back-Illuminated 6 μm SPAD Depth Sensor with PDE 36.5% at 940 nm Via Combination of Dual Diffraction Structure and 2×2 On-Chip Lens 249
Y. Fujisaki, H. Tsugawa, K. Sakai, H. Kumagai, R. Nakamura, T. Ogita, S. Endo, T. Iwase, H. Takase, K. Yokochi, S. Yoshida, S. Shimada, Y. Otake, T. Wakano, H. Hiyama, K. Hagiwara, M. Arakawal, S. Matsumotol, H. Maeda, K. Sugihara, K. Takabayashi, M. Ono, K. Ishibashi, K. Yamamoto

Human Activity Recognition SoC for AR/VR with Integrated Neural Sensing, AI Classifier and Chained Infrared Communication for Multi-Chip Collaboration 251
Yijie Wei, Xi Chen, Jie Gu

216 fps 672 × 512 Pixel 3 μm Indirect Time-Of-Flight Image Sensor with 1-Frame Depth Acquisition for Motion Artifact Suppression 253
Chihiro Okada, Sozo Yokogawa, Yuhi Yorikado, Katsumi Honda, Naoki Okuno, Ryohei Ikeno, Makoto Yamakoshi, Hiroshi Ito, Shohei Yoshitsune, Masatsugu Desaki, Shota Hida, Atsushi Nose, Hayato Wakabayashi, Fumihiko Koga

A 3.96μm, 124dB Dynamic Range, 6.2mW Stacked Digital Pixel Sensor with Monochrome and Near-Infrared Dual-Channel Global Shutter Capture 255
Song Chen, Chiao Liu, Lyle Bainbridge, Qing Chao, Ramakrishna Chilukuri, Wei Gao, Andrew P. Hammond, Tsung-Hsun Tsai, Ken Miyauchi, Isao Takayanagi, Masato Nagamatsu, Hirofumi Abe, Kazuya Mori, Masayuki Uno, Toshiyuki Isozaki, Rimon Ikeno, Hsin-Li Chen, Chih-Hao Lin, Wen-Chien Fu, Shou-Gwo Wuu

Doping-Optimized Back-Illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm 257
Eunsung Park, Won-Yong Ha, Doyoon Eom, Dae-Hwan Ahn, Hyuk An, Suhyun Yi, Kyung-Do Kim, Jongchae Kim, Woo-Young Choi, Myung-Jae Lee

AMD Instinct™ MI250X Accelerator Enabled by Elevated Fanout Bridge Advanced Packaging Architecture 259
Raja Swaminathan, Michael J. Schulte, Brett Wilkerson, Gabriel H. Loh, Alan Smith, Norman James

An Integrated System Scaling Solution for Future High Performance Computing 261
Chih-Hang Tung, Doug C. H. Yu

4-Layer Wafer on Wafer Stacking Demonstration with Face to Face/Face to Back Stacked Flexibility Using Hybrid Bond/TSV-Middle for Various 3D Integration 263
C.-L. Lu, C.-H. Chuang, C.-H. Huang, S.-C. Lin, Y.-H. Chang, W.-Y. Lai, M.-H. Chiu, M.-H. Liao, S.-Z. Chang

Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy 265
Norio Chujo, Koji Sakui, Shinji Sugatani, Hiroyuki Ryoson, Tomoji Nakamura, Takayuki Ohba

1Mbit 1T1C 3D DRAM with Monolithically Stacked One Planar FET and Two Vertical FET Heterogeneous Oxide Semiconductor Layers Over Si CMOS 267
Y. Okamoto, Y. Komura, T. Mizuguchi, T. Saito, M. Ito, K. Kimura, T. Onuki, Y. Ando, H. Sawai, T. Murakawa, H. Kunitake, T. Matsuzaki, H. Kimura, M Fujita, M Ikeda, S. Yamazaki

How Harsh is Space?–Equations that Connect Space and Ground VLSI 269
Daisuke Kobayashi, Kazuyuki Hirose

Enabling High-Speed, High-Resolution Space-Based Focal Plane Arrays with Analog In-Memory Computing 271
T. P. Xiao, W. S. Wahby, C. H. Bennett, P. Hays, V. Agrawal, M. J. Marinella, S. Agarwal

ASIL-D Automotive-Grade Microcontroller in 28nm FD-SOI with full-OTA Capable 21MB Embedded PCM Memory and Highly Scalable Power Management 273
N. Grossier, F. Disegni, A. Ventre, A. Barcella, R. Mariani, V. Marino, S. Mazzara, A. Scavuzzo, M. Bansal, B. Soni, A. Anand, S. Banzal, D. Joshi, R. Narwal, M. Niranjani, K. Trivedi, P. Ferreira, R. Ranica, L. Vullo, A. Cathelin, A. Maurelli, S. Pezzini, M. Peri

Multi-Chiplet Heterogeneous Integration Packaging for Semiconductor System Scaling 275
Surya Bhattacharya, Vempati Srinivasa Rao

A Six-Word Story on the Future of VLSI: AI-Driven, Software-Defined, and Uncomfortably Exciting 279
Parthasarathy Ranganathan

Quantum Computing from Hype to Game Changer 283
Hiroyuki Mizuno

Searching for Nonlinearity: Scaling Limits in NAND Flash 287
Siva Sivaram, Alper Ilkbahar

E-Core Implementation in Intel 4 with PowerVia (Backside Power) Technology 291
M. Shamanna, E. Abuayob, G. Aenuganti, C. Alvares, J. Antony, A. Bahudhanam, A. Chandran, P. Chew, A. Chatterjee, B. Chauhan, N. Dandeti, J. Desai, M. Doyle, T. Dmukauskas, P. Farache, E. Fetzer, K. Fischer, P. Hack, Y. Greenzweig, J. Giacobbe, W. Hafez, E. Haralson, A. Hegde, A. Illa, M. Islam, S. Jain, M. Jang, J. Nguyen, T. Tong, L. Jiang, E. Karl, P. Kalangi, G. Khoo, A. Krishnamoorthy, B. Kuns, W. Li, R. Livengood, T. Malik, R. Priyanka, H. Faraby, Y. Maymon, K. Mistry, K. Morgan, S. Natarajan, O. Nevo, M. Oh, P. Pardy, J. Park, P. Penmatsa, B. Phelps, C. Peterson, S. Rajappa, A. Raveh, A Rezaie, T. Ravishankar, R. Ramaswamy, S. Reddy, R. Saha, S. Sen, R. Sanchez, R. Sanaga, B. Simkhovich, B. Sell, M. Senger, B. Schnarch, M. Seshadri, O. Sidorov, S. Subramaniam, K. Subramanian, B. Truong, S. Bangalore, J. Hicks, S. Venkatesh, D. Christensen, K. Bhargav, M. Von Haartman, P. Joshi, S. Zickel, C-H Lin, J. Huening, T-H Wu, N. Bakken, A. Afzal, A. Raman, Sj. Rao, V. Kawar, J. Neirynck, D. Bradley, M. Duwe, S. Wu, V. Patil, M. Bayoumy

World's First GAA 3nm Foundry Platform Technology (SF3) with Novel Multi-Bridge-Channel-FET (MBCFET™) Process 293
Jaehun Jeong, Sang Hyeon Lee, Sada-Aki Masuoka, Shincheol Min, Sanghoon Lee, Seungkwon Kim, Taehun Myung, Byungha Choi, Chang-Woo Sohn, Sung Won Kim, Jeongmin Choi, Jungmin Park, Hyungjong Lee, Taeyoung Kim, Seokhoon Kim, Yuri Yasuda-Masuoka, Ja-Hum Ku, Gitae Jeong

Nanosheet-Based Complementary Field-Effect Transistors (CFETs) at 48nm Gate Pitch, and Middle Dielectric Isolation to Enable CFET Inner Spacer Formation and Multi-Vt Patterning 295
H. Mertens, M. Hosseini, T. Chiarella, D. Zhou, S. Wang, G. Mannaert, E. Dupuy, D. Radisic, Z. Tao, Y. Oniki, A. Hikavyy, R. Rosseel, A. Mingardi, S. Choudhury, P. Puttarame Gowda, F. Sebaai, A. Peter, K. Vandersmissen, J. P. Soulie, A. De Keersgieter, L. Petersen Barbosa Lima, C. Cavalcante, D. Batuk, G. T. Martinez, J. Geypen, F. Seidel, K. Paulussen, P. Favia, J. Boemmels, R. Loo, P. Wong, A. Sepulveda Marquez, B. T. Chan, J. Mitard, S. Subramanian, S. Demuynck, E. Dentoni Litta, N. Horiguchi, S. Samavedam, S. Biesemans

Scaled Contact Length with Low Contact Resistance in Monolayer 2D Channel Transistors 297
Wen-Chia Wu, Terry Y. T. Hung, D. Mahaveer Sathaiya, Dongxu Fan, Goutham Arutchelvan, Chen-Feng Hsu, Sheng-Kai Su, Ang Sheng Chou, Edward Chen, Weisheng Li, Zhihao Yu, Hao Qiu, Ying-Mei Yang, Kuang-I Lin, Yun-Yang Shen, Wen-Hao Chang, San Lin Liew, Vincent Hou, Jin Cai, Chung-Cheng Wu, Jeff Wu, H.-S. Philip Wong, Xinran Wang, Chao-Hsin Chien, Chao-Ching Cheng, Iuliana P. Radu

Contact Cavity Shaping and Selective SiGe:B Low-Temperature Epitaxy Process Solution for Sub 10^{-9} $\Omega.cm^2$ Contact Resistivity in Nonplanar FETs 299
N. Breil, B-C. Lee, J. Avila Avendano, J. Jewell, M. Vellaikal, E. Newman, E. M. Bazizi, A. Pal, L. Liu, O. Gluschenkov, A. Greene, S. Mochizuki, N. Loubet, B. Colombeau, B. Haran

Novel Bridge Transmission Line Method for Thin-Film Semiconductors: Modelling, Simulation Verification, and Experimental Demonstration 301
Kaizhen Han, Yuye Kang, Yue Chen, Xiao Gong

First Study of the Charge Trapping Aggravation Induced by Anti-Ferroelectric Switching in the MFIS Stack 303
Zuopu Zhou, Leming Jiao, Zijie Zheng, Xiaolin Wang, Dong Zhang, Kai Ni, Xiao Gong

Catching the Missing EM Consequence in Soft Breakdown Reliability in Advanced FinFETs: Impacts of Self-Heating, On-State TDDB, and Layout Dependence 305
Zuoyuan Dong, Zixuan Sun, Xin Yang, Xiaomei Li, Yongkang Xue, Chen Luo, Puyang Cai, Zirui Wang, Shuying Wang, Yewei Zhang, Chaolun Wang, Pengpeng Ren, Zhigang Ji, Xing Wu, Runsheng Wang, Ru Huang

FeRAM Recovery Up to 200 Periods with Accumulated Endurance 10^{12} Cycles and an Applicable Array Circuit Toward Unlimited eNVM Operations 307
K.-Y. Hsiang, J.-Y. Lee, F.-S. Chang, Z.-F. Lou, Z.-X. Li, Z.-H. Li, J.-H. Chen, C. W. Liu, T.-H. Hou, M. H. Lee

Novel Strategies for Highly Uniform and Reliable Cell Characteristics of 8th Generation 1Tb 3D-NAND Flash Memory 309
Changhwan Lee, Min-Tai Yu, Sejun Park, Hoki Lee, Bio Kim, Suhwan Lim, Jaeduk Lee, Sung-Hun Lee, Mincheol Park, Su Jin Ahn, Sung Hoi Hur

Beyond 10 μm Depth Ultra-High Speed Etch Process with 84% Lower Carbon Footprint for Memory Channel Hole of 3D NAND Flash Over 400 Layers 311
Yoshihide Kihara, Maju Tomura, Wataru Sakamoto, Masanobu Honda, Masayuki Kojima

Demonstration of Recovery Annealing on 7-Bits Per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability 313
Yuta Aiba, Yusuke Higashi, Hitomi Tanaka, Hiroki Tanaka, Fumie Kikushima, Toshio Fujisawa, Hideko Mukaida, Masayuki Miura, Tomoya Sanuki

High Bit Cost Scalability and Reliable Cell Characteristics for 7th Generation 1Tb 4Bit/Cell 3D-NAND Flash 315
Kyungmoon Kim, Yujeong Seo, Sejun Park, Woojae Jang, Dongho Yoo, Joonsung Lim, Il-Han Park, Jaeduk Lee, Kyungyoon Noh, Sujin Ahn, Sunghoi Hur

Breakthrough Design Technology Co-Optimization Using BSPDN and Standard Cell Variants for Maximizing Block-Level PPA 317
Seungyoung Lee, Sungyup Jung, Yunkyeong Jang, Jungho Do, Jisu Yu, Hyeoungyu You, Minjae Jeong, Jinyoung Lim, Jiyun Han, Sangdo Park, Yongdeok Kim, Jooyeon Kwon, Hoonki Kim, Seiseung Yoon

PPA and Scaling Potential of Backside Power Options in N2 and A14 Nanosheet Technology 319
S. Yang, P. Schuddinck, M. Garcia-Bardon, Y. Xiang, A. Veloso, B T Chan, G. Mirabelli, G. Hiblot, G. Hellings, J. Ryckaert

Upcoming Challenges of ESD Reliability in DTCO with BS-PDN Routing Via BPRs 321
W.-C. Chen, S.-H. Chen, A. Veloso, K. Serbulova, G. Hellings, G. Groeseneken

Towards DTCO in High Temperature GaN-On-Si Technology: Arithmetic Logic Unit at 300 °C and CAD Framework Up to 500 °C 323
Qingyun Xie, Mengyang Yuan, John Niroula, Bejoy Sikder, Shisong Luo, Kai Fu, Nitul S. Rajput, Ayan Biswas Pranta, Pradyot Yadav, Yuji Zhao, Nadim Chowdhury, Tomás Palacios

Strategy for 3D Ferroelectric Transistor: Critical Surface Orientation Dependence of $HfZrO_x$ on Si 325
Song-Hyeon Kuk, Jae-Hoon Han, Bong Ho Kim, Joon Pyo Kim, Sang-Hyeon Kim

HZO Scaling and Fatigue Recovery in FeFET with Low Voltage Operation: Evidence of Transition from Interface Degradation to Ferroelectric Fatigue 327
Zuocheng Cai, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi

First Stacked Nanosheet FeFET Featuring Memory Window of 1.8V at Record Low Write Voltage of 2V and Endurance >1E11 Cycles 329
Yu-Rui Chen, Yi-Chun Liu, Zefu Zhao, Wan-Hsuan Hsieh, Jia-Yang Lee, Chien-Te Tu, Bo-Wei Huang, Jer-Fu Wang, Shee-Jier Chueh, Yifan Xing, Guan-Hua Chen, Hung-Chun Chou, Dong Soo Woo, M. H. Lee, C. W. Liu

First Demonstration of BEOL-Compatible MFMIS Fe-FETs with 3D Multi-Fin Floating Gate: In-Situ ALD-Deposited MFM, L_{CH} of 50 Nm,> 2×10^9 Endurance, and 58.3% Area Saving 331
Xiaolin Wang, Zijie Zheng, Qiwen Kong, Leming Jiao, Kaizhen Han, Chen Sun, Zuopu Zhou, Long Liu, Yuye Kang, Gan Liu, Dong Zhang, Xiao Gong

Cold-FeFET as Embedded Non-Volatile Memory with Unlimited Cycling Endurance 333
Sharadindu Gopal Kirtania, Khandker Akif Aabrar, Asif I. Khan, Shimeng Yu, S. Datta

Intel PowerVia Technology: Backside Power Delivery for High Density and High-Performance Computing 335
W. Hafez, P. Agnihotri, M. Asoro, M. Aykol, B. Bains, R. Bambery, M. Bapna, A. Barik, A. Chatterjee, P. C. Chiu, T. Chu, C. Firby, K. Fischer, M. Fradkin, H. Greve, A. Gupta, E. Haralson, M. Haran, J. Hicks, A. Illa, M. Jang, S. Klopcic, M. Kobrinsky, B. Kuns, H.-H. Lai, G. Lanni, S.-H. Lee, N. Lindert, C.-L. Lo, Y. Luo, G. Malyavanatham, B. Marinkovic, Y. Maymon, M. Nabors, J. Neirynck, P. Packan, A. Paliwal, L. Pantisano, L. Paulson, P. Penmatsa, C. Prasad, C. Puls, T. Rahman, R. Ramaswamy, S. Samant, B. Sell, K. Sethi, F. Shah, M. Shamanna, K. Shang, Q. Li, M. Sibakoti, J. Stoeger, N. Strutt, R. Thirugnanasambandam, C. Tsai, X. Wang, A. Wang, S.-J. Wu, Q. Xu, X.-H. Zhong, S. Natarajan

High Performance 5G Mobile SOC Productization with 4nm EUV Fin-FET Technology 337
Jun Yuan, Jie Deng, Vicki Lin, Ying Chen, Joseph Chiu, Minghuei Lin, Jun Chen, Deedee Zhang, Yukai Chen, David Liu, Bo Yu, Hao Wang, Giri Nallapati, Vivek Mohan, Venu Sanaka, Berkan Baran, Frank Dahan, Prasad Bhadri, Rajesh Geol, Venu Boynapalli, Seyfi Bazarjani, Paul Penzes, Parag Agashe, P. R. Chidambaram

Molybdenum Nitride as a Scalable and Thermally Stable pWFM for CFET 339
H. Arimura, S. Brus, J. Franco, Y. Oniki, A. Vandooren, T. Conard, B.-T. Chan, B. Kannan, M. Samiee, W. Li, P. Deminskyi, E. Shero, J. Bakke, N. Jourdan, G. Alessio Verni, J. W. Maes, M. Givens, L.-å. Ragnarsson, J. Mitard, E. Dentoni Litta, N. Horiguchi

Integration of a Stacked Contact MOL for Monolithic CFET 341
Victor Vega-Gonzalez, D. Radisic, BT Chan, S. Choudhury, S. Wang, A. Mingardi, Q. Toan Le, H. Decoster, Y. Oniki, P. Puttarame, K. Vandersmissen, J.-P. Soulie, A. Peter, A. Sepulveda. D. Batuk, G. T. Martinez, O. Richard, J. Boemmels, S. Biesemans, E. Dentoni, N. Horiguchi, S. Park, Z. Tokei

Front-Side and Back-Side Power Delivery Network Guidelines for 2nm Node High Perf Computing and Mobile SoC Applications 343
J. Lee, J. Jeong, S. Lee, S. Lee, J. Lim, S. C. Song, S. Ekbote, N. Stevens-Yu, D. Greenlaw, R.-H. Baek

Highly Scalable Metal Induced Lateral Crystallization (MILC) Techniques for Vertical Si Channel in Ultra-High (> 300 Layers) 3D Flash Memory 345
N. Ishihara, Y. Shimada, T. Ochi, S. Seto, H. Matsuo, H. Yamashita, S. Morita, M. Ukishima, K. Uejima, Y. Arayashiki, S. Kajiwara, A. Murayama, K. Nishiyama, K. Sugimae, S. Mori, Y. Saito, T. Shundo, A. Maeda, H. Kamiya, Y. Uchiyama, M. Fujiwara, F. Aiso, K. Sekine, N. Ohtani

QLC Programmable 3D Ferroelectric NAND Flash Memory by Memory Window Expansion Using Cell Stack Engineering 347
Sunghyun Yoon, Sung-In Hong, Daehyun Kim, Garam Choi, Young Mo Kim, Kyunghoon Min, Seiyon Kim, Myung-Hee Na, Seonyong Cha

First Observation of Ultra-High Polarization (~ 108 μC/cm²) in Nanometer Scaled High Performance Ferroelectric HZO Capacitors with Mo Electrodes 349
F. Huang, B. Saini, L. Wan, H. Lu, X. He, S. Qin, W. Tsai, A. Gruverman, A. C. Meng, H.-S. P. Wong, P. C. McIntyre, S. S. Wong

Noise Performance Improvements of 2-Layer Transistor Pixel Stacked CMOS Image Sensor with Non-Doped Pixel-FinFETs 351
Y. Kikuchi, M. Tomita, T. Hayashi, H. Chiba, T. Ogita, T. Okawa, K. Nishida, M. Sugimoto, D. Yoneyama, T. Umeki, H. Oishi, S. Miyake, K. Hiramatsu, H. Kumano, H. Kawashima, N. Yamada, M. Tamura, H. Ohnuma, K. Tatani

Cryogenic RF Transistors and Routing Circuits Based on 3D Stackable InGaAs HEMTs with Nb Superconductors for Large-Scale Quantum Signal Processing 353
Jaeyong Jeong, Seong Kwang Kim, Yoon-Je Suh, Jisung Lee, Joonyoung Choi, Juhyuk Park, Joon Pyo Kim, Bong Ho Kim, Younjung Jo, Seung-Young Park, Jongmin Kim, Sanghyeon Kim

Building High Performance Transistors on Carbon Nanotube Channel 355
Gregory Pitner, Nathaniel Safron, Tzu-Ang Chao, Shengman Li, Sheng-Kai Su, Gilad Zeevi, Qing Lin, Hsin-Yuan Chiu, Matthias Passlack, Zichen Zhang, D. Mahaveer Sathaiya, Aslan Wei, Carlo Gilardi, Edward Chen, San-Lin Liew, Vincent D.-H. Hou, Chung-Wei Wu, Jeff Wu, Zhiwei Lin, Jeffrey Fagan, Ming Zheng, Han Wang, Subhasish Mitra, H.-S. Philip Wong, Iuliana Radu

Record High Active Boron Doping Using Low Temperature In-Situ CVD: Enabling Sub-5×10^{-10} Ω-cm^2 ρ_c from Cryogenic (5 K) to Room Temperature 357
Gerui Zheng, Yuxuan Wang, Haiwen Xu, Rami Khazaka, Lutz Muehlenbein, Sheng Luo, Xuanqi Chen, Rui Shao, Zijie Zheng, Gengchiau Liang, Xiao Gong

L_g = 60 nm $In_{0.53}Ga_{0.47}As$ MBCFETs: From G_{m_max} = 13.7 mS/μm and Q = 180 to Virtual-Source Modeling 359
J.-H. Yoo, H.-B. Jo, I.-G. Lee, S.-M. Choi, J.-M. Baek, S T. Lee, H. Jang, M W. Kong, H H. Kim, H J. Lee, H.-J. Kim, H.-S. Jeong, W.-S. Park, D H. Ko, S. H. Shin, H.-M. Kwon, S K. Kim, J G. Kim, J. Yun, T. Kim, K.-Y. Shin, T.-W. Kim, J.-K. Shin, J.-H. Lee, C.-S. Shin, K.-S. Seo, D.-H. Kim

High Performance 5 nm Si Nanowire FETs with a Record Small SS = 2.3 mV/dec and High Transconductance at 5.5 K Enabled by Dopant Segregated Silicide Source/Drain 361
Yi Han, Jingxuan Sun, Jin-Hee Bae, Detlev Grützmacher, Joachim Knoch, Qing-Tai Zhao

The Chalcogenide-Based Memory Technology Continues: Beyond 20nm 4-Deck 256Gb Cross-Point Memory 363
Jaeyun Yi, Myoungsub Kim, Jungwon Seo, Namkyun Park, Seungyun Lee, Jongil Kim, Gapsok Do, Hongjin Jang, Hyochol Koo, Sunglae Cho, Sujin Chae, Taehoon Kim, Myung-Hee Na, Seonyong Cha

Simple Binary In-Te OTS with Sub-Nm HfO_x Buffer Layer for 3D Vertical X-Point Memory Applications 365
Sanghyun Ban, Jangseop Lee, Taehoon Kim, Hyunsang Hwang

16-Layer 3D Vertical RRAM with Low Read Latency (18ns), High Nonlinearity (>5000) and Ultra-Low Leakage Current (~pA) Self-Selective Cells 367
Yaxin Ding, Jianguo Yang, Yu Liu, Jianfeng Gao, Yuan Wang, Pengfei Jiang, Shuxian Lv, Yuting Chen, Boping Wang, Wei Wei, Tiancheng Gong, Kan-Hao Xue, Qing Luo, Xiangshui Miao, Ming Liu

High Density Embedded 3D Stackable Via RRAM in Advanced MCU Applications 369
Yao-Hung Huang, Yu-Cheng Hsieh, Yu-Cheng Lin, Yue-Der Chih, Eric Wang, Jonathan Chang, Ya-Chin King, Chrong Jung Lin

First Demonstration of a Design Methodology for Highly Reliable Operation at High Temperature on 128kb 1T1C FeRAM Chip 371
Tiancheng Gong, Lihua Xu, Wei Wei, Pengfei Jiang, Peng Yuan, Bowen Nie, Yuanquan Huang, Yuan Wang, Yang Yang, Jianfeng Gao, Junfeng Li, Jun Luo, Lingfei Wang, Jianguo Yang, Qing Luo, Ling Li, Steve S. Chung, Ming Liu

3D Stackable Vertical Ferroelectric Tunneling Junction (V-FTJ) with On/Off Ratio 1500x, Applicable Cell Current, Self-Rectifying Ratio 1000x, Robust Endurance of 10^9 Cycles, Multilevel and Demonstrated Macro Operation Toward High-Density BEOL NVMs 373
J.-Y. Lee, F.-S. Chang, K.-Y. Hsiang, P.-H. Chen, Z.-F. Luo, Z.-X. Li, J.-H. Tsai, C. W. Liu, M. H. Lee

Ultra-High Tunneling Electroresistance Ratio (2×10^4) & Endurance (10^8) in Oxide Semiconductor-Hafnia Self-Rectifying (1.5×10^3) Ferroelectric Tunnel Junction 375
Junghyeon Hwang, Chaeheon Kim, Hunbeom Shin, Hwayoung Kim, Sang-Hee Ko Park, Sanghun Jeon

First Demonstration of BEOL-Compatible Write-Enhanced Ferroelectric-Modulated Diode (FMD): New Possibility for Oxide Semiconductor Memory Devices 377
Leming Jiao, Kaizhen Han, Zuopu Zhou, Zijie Zheng, Xiaolin Wang, Qiwen Kong, Yuye Kang, Jishen Zhang, Long Liu, Xiao Gong

Ultrathin Atomic-Layer-Deposited In_2O_3 Radio-Frequency Transistors with Record High f_T of 36 GHz and BEOL Compatibility 379
Dongqi Zheng, Adam Charnas, Jian-Yu Lin, Jackson Anderson, Dana Weinstein, Peide D. Ye

Thickness-Engineered Extremely-Thin Channel High Performance ITO TFTs with Raised S/D Architecture: Record-Low R_{SD}, Highest Moblity (Sub-4 nm T_{CH} Regime), and High V_{TH} Tunability 381
Yuye Kang, Kaizhen Han, Yue Chen, Xiao Gong

Ultrahigh Bias Stability of ALD In_2O_3 FETs Enabled by High Temperature O_2 Annealing 383
Zhuocheng Zhang, Zehao Lin, Chang Niu, Mengwei Si, Muhammad A. Alam, Peide D. Ye

Co-Designed Capacitive Coupling-Immune Sensing Scheme for Indium-Tin-Oxide (ITO) 2T Gain Cell Operating at Positive Voltage Below 2 V 385
Kasidit Toprasertpong, Shuhan Liu, Jian Chen, Sumaiya Wahid, Koustav Jana, Wei-Chen Chen, Shengman Li, Eric Pop, H.-S. Philip Wong

Grain Size Reduction of Ferroelectric HZO Enabled by a Novel Solid Phase Epitaxy (SPE) Approach: Working Principle, Experimental Demonstration, and Theoretical Understanding 387
Dong Zhang, Jixuan Wu, Qiwen Kong, Zuopu Zhou, Long Liu, Kaizhen Han, Chen Sun, Xiaolin Wang, Gan Liu, Leming Jiao, Zijie Zheng, Yuye Kang, Jiezhi Chen, Xiao Gong

First Demonstration of Work Function-Engineered BEOL-Compatible IGZO Non-Volatile MFMIS AFeFETs and Their Co-Integration with Volatile-AFeFETs 389
Zijie Zheng, Leming Jiao, Zuopu Zhou, Yuxuan Wang, Long Liu, Kaizhen Han, Chen Sun, Qiwen Kong, Dong Zhang, Xiaolin Wang, Kai Ni, Xiao Gong

Record Transconductance in L_{eff}~30 nm Self-Aligned Replacement Gate ETSOI nFETs Using Low EOT Negative Capacitance HfO_2-ZrO_2 Superlattice Gate Stack 391
L.-C. Wang, W. Li, N. Shanker, S. S. Cheema, S.-L. Hsu, S. Volkman, U. Sikder, C. Garg, J.-H. Park, Y.-H. Liao, Y.-K. Lin, C. Hu, S. Salahuddin

Towards Epitaxial Ferroelectric HZO on n^+-Si/Ge Substrates Achieving Record $2P_r = 84\ \mu C/cm^2$ and Endurance > 1E11 393
Zefu Zhao, Yu-Rui Chen, Yun-Wen Chen, Wan-Hsuan Hsieh, Jer-Fu Wang, Jia-Yang Lee, Yifan Xing, Guan-Hua Chen, C. W. Liu

Comprehensive 300 mm Process for Silicon Spin Qubits with Modular Integration 395
A. Elsayed, C. Godfrin, N. I. Dumoulin Stuyck, M. M. K. Shehata, S. Kubicek, S. Massar, Y. Canvel, J. Jussot, A. Hikavyy, R. Loo, G. Simion, M. Mongillo, D. Wan, B. Govoreanu, R. Li, I. P. Radu, P. Van Dorpe, K. De Greve

Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control 397
Fabio Bersano, Michele Aldeghi, Eloi Collette, Michele Ghini, Franco De Palma, Fabian Oppliger, Pasquale Scarlino, Floris Braakman, Martino Poggio, Heike Riel, Gian Salis, Rolf Allenspach, Adrian M. Ionescu

How Fault-Tolerant Quantum Computing Benefits from Cryo-CMOS Technology 399
H.-L. Chiang, R. A. Hadi, J.-F. Wang, H.-C. Han, J.-J. Wu, H.-H. Hsieh, J.-J. Horng, W.-S. Chou, B.-S. Lien, C.-H. Chang, Y.-C. Chen, Y.-H. Wang, T.-C. Chen, J.-C. Liu, Y.-C. Liu, M.-H. Chiang, K.-H. Kao, B. Pulicherla, J. Cai, C.-S. Chang, K.-W. Su, K.-L. Cheng, T.-J. Yeh, Y.-C. Peng, C. Enz, M.-C. F. Chang, M.-F. Chang, H.-S. P. Wong, I. P. Radu

Determining the Low-Frequency Noise Source in Cryogenic Operation of Short-Channel Bulk MOSFETs 401
Takumi Inaba, Hiroshi Oka, Hidehiro Asai, Hiroshi Fuketa, Shota Iizuka, Kimihiko Kato, Shunsuke Shitakata, Koichi Fukuda, Takahiro Mori

A Nanosheet Oxide Semiconductor FET Using ALD InGaOx Channel and InSnOx Electrode with Normally-Off Operation, High Mobility and Reliability for 3D Integrated Devices 403
Kaito Hikake, Zhuo Li, Junxiang Hao, Chitra Pandy, Takuya Saraya, Toshiro Hiramoto, Takanori Takahashi, Mutsunori Uenuma, Yukiharu Uraoka, Masaharu Kobayashi

Aggressively Scaled Atomic Layer Deposited Amorphous $InZnO_x$ Thin Film Transistor Exhibiting Prominent Short Channel Characteristics (SS= 69 mV/dec.; DIBL = 27.8 mV/V) and High G_m (802 μS/μm at V_{DS} = 2V) 405
Yan-Kui Liang, June-Yang Zheng, Yu-Lon Lin, Wei-Li Li, Yu-Cheng Lu, Dong-Ru Hsieh, Li-Chi Peng, Tsung-Te Chou, Chi-Chung Kei, Chun-Chieh Lu, Huai-Ying Huang, Yuan-Chieh Tseng, Tien-Sheng Chao, Edward Yi Chang, Chun-Hsiung Lin

2D Materials in the BEOL 407
C. H. Naylor, K. Maxey, C. Jezewski, K. P. O'Brien, A. V. Penumatcha, M. S. Kavrik, B. Agrawal, C. V. Littlefield, J. Lux, B. Barley, J. R. Weber, A. Sen Gupta, C. J. Dorow, N. Arefin, S. King, R. Chebiam, J. Plombon, S. B. Clendenning, U. E. Avci, M. Kobrinsky, M. Metz

Integration of Epitaxial Monolayer MX_2 Channels on 300mm Wafers Via Collective-Die-To-Wafer (CoD2W) Transfer 409
S. Ghosh, Q. Smets, S. Banerjee, T. Schram, K. Kennes, R. Verheyen, P. Kumar, M.-E. Boulon, B. Groven, H. M. Silva, S. Kundu, D. Cott, D. Lin, P. Favia, T. Nuytten, A. Phommahaxay, I. Asselberghs, C. De La Rosa, G. S. Kar, S. Brems

Towards Low Damage and Fab-Compatible Top-Contacts in MX_2 Transistors Using a Combined Synchronous Pulse Atomic Layer Etch and Wet-Chemical Etch Approach 411
S. Kundu, D. H. Van Dorp, T. Schram, Q. Smets, S. Banerjee, B. Groven, D. Cott, S. Decoster, P. Bezard, F. Lazzarino, K. Banerjee, S. Ghosh, J. F. De Marneffe, P. Morin, C. J. L. De La Rosa, I. Asselberghs, G. S. Kar

Chip Demonstration of a High-Density (43Gb) and High-Search-Bandwidth (300Gb/s) 3D NAND Based In-Memory Search Accelerator for Ternary Content Addressable Memory (TCAM) and Proximity Search of Hamming Distance 413
Chih-Chang Hsieh, Hang-Ting Lue, Yung-Chun Li, Shuo-Nan Hung, Chun-Hsiung Hung, Keh-Chung Wang, Chih-Yuan Lu

3-Bits-Per-Cell $2T32C_{FE}$ nvTCAM by Angstrom-Laminated Ferroelectric Layers with 10^{11} Cycles of Endurance and 4.92V of Ultra-Wide Memory-Windows for In-Memory-Searching 415
E. R. Hsieh, Y. T. Tang, C. R. Liu, S. M. Wang, Y. L. Hsueh, R. Q. Lin, Y. X. Huang, Y. T. Chen

Write-Enhanced Single-Ended 11T SRAM Enabling Single Bitcell Reconfigurable Compute-In-Memory Employing Complementary FETs 417
Wei-Xiang You, Cheng-Yin Wang, Yih Wang, Tsung-Yung Jonathan Chang, Szuya Sandy Liao

Monolithic 3D Integration of FeFET, Hybrid CMOS Logic and Analog RRAM Array for Energy-Efficient Reconfigurable Computing-In-Memory Architecture 419
Yiwei Du, Jianshi Tang, Yijun Li, Yue Xi, Bin Gao, He Qian, Huaqiang Wu

Characterizing and Reducing the Layout Dependent Effect and Gate Resistance to Enable Multiple-Vt Scaling for a 3nm CMOS Technology 421
C. A. Lu, H. P. Lee, H. C. Chen, Y. C. Lin, Y. H. Chung, S. H. Wang, J. Y. Yeh, V. S. Chang, M. C. Chiang, W. Chang, H. C. Chung, C. F. Cheng, H. H. Hsu, H. H. Liu, William P. N. Chen, C. Y. Lin

Novel Low Thermal Budget CMOS RMG: Performance and Reliability Benchmark Against Conventional High Thermal Budget Gate Stack Solutions 423
J. Franco, H. Arimura, J.-F. De Marneffe, S. Brus, R. Ritzenthaler, E. Dentoni Litta, K. Croes, B. Kaczer, N. Horiguchi

Highly Reliable/Manufacturable 4nm FinFET Platform Technology (SF4X) for HPC Application with Dual-CPP/HP-HD Standard Cells 425
Kihwang Son, Seulki Park, Kyunghoon Jung, Jun-Gyu Kim, Younggun Ko, Keonyong Cheon, Changkeun Yoon, Jiho Kim, Jaehun Jeong, Taehun Myung, Changmin Hong, Weonwi Jang, Min-Chul Sun, Sungil Jo, Ju-Youn Kim, Byungmoo Song, Yuri Yasuda-Masuoka, Ja-Hum Ku, Gitae Jeong

Extremely High-κ $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs Featuring Respective Record I_{ON} Per Footprint of 9200μA/μm and Record I_{ON} Per Stack of 360μA at $V_{OV}=V_{DS}=0.5V$ 427
Yi-Chun Liu, Yu-Rui Chen, Yun-Wen Chen, Hsin-Cheng Lin, Wan-Hsuan Hsieh, Chien-Te Tu, Bo-Wei Huang, Wei-Jen Chen, Chun-Yi Cheng, Shee-Jier Chueh, C. W. Liu

Overcoming Negative nFET V_{TH} by Defect-Compensated Low-Thermal Budget ITO-IGZO Hetero-Oxide Channel to Achieve Record Mobility and Enhancement-Mode Operation 429
Sonu Hooda, Chun-Kuei Chen, Manohar Lal, Shih-Hao Tsai, Evgeny Zamburg, Aaron Voon-Yew Thean

First Demonstration of BEOL-Compatible Atomic-Layer-Deposited InGaZnO TFTs with 1.5 nm Channel Thickness and 60 nm Channel Length Achieving ON/OFF Ratio Exceeding 10^{11}, SS of 68 mV/dec, Normal-Off Operation and High Positive Gate Bias Stability 431
Jie Zhang, Zhuocheng Zhang, Zehao Lin, Ke Xu, Hongyi Dou, Bo Yang, Xinghang Zhang, Haiyan Wang, Peide D. Ye

First Demonstration of a-IGZO GAA Nanosheet FETs Featuring Achievable SS=61mV/dec,I_{off} <10^{-7} μA/μm, DIBL =44mV/V, Positive V_T, and Process Temp. of 300 °C 433
Jih-Chao Chiu, Eknath Sarkar, Yuan-Ming Liu, Yu-Ciao Chen, Yu-Cheng Fan, C. W. Liu

Demonstration of Crystalline IGZO Transistor with High Thermal Stability for Memory Applications 435
Whayoung Kim, Jaehyeon Kim, Dongjin Ko, Jun-Hwe Cha, Gyeongcheol Park, Youngbae Ahn, Jong-Young Lee, Minchul Sung, Hyejung Choi, Seung Wook Ryu, Seiyon Kim, Myunghee Na, Seonyong Cha

Lowest $I_{OFF} < 3\times10^{-21}$ A/μm in Capacitorless DRAM Achieved by Reactive Ion Etch of IGZO-TFT 437
A. Belmonte, S. Kundu, S. Subhechha, A. Chasin, N. Rassoul, H. Dekkers, H. Puliyalil, F. Seidel, P. Carolan, R. Delhougne, G. S. Kar

14nm DRAM Development and Manufacturing 439
Kanguk Kim, Youngwoo Son, Hoin Ryu, Byunghyun Lee, Jooncheol Kim, Hyunsu Shin, Joonyoung Kang, Jihun Kim, Shinwoo Jeong, Kyosuk Chae, Dongkak Lee, Ilwoo Jung, Yongkwan Kim, Boyoung Song, Jeonghoon Oh, Jungwoo Song, Seguen Park, Keumjoo Lee, Hyodong Ban, Jiyoung Kim, Jooyoung Lee

A 135 GBps/Gbit 0.66 pJ/bit Stacked Embedded DRAM with Multilayer Arrays by Fine Pitch Hybrid Bonding and Mini-TSV 441
Song Wang, Bing Yu, Wenwu Xiao, Fujun Bai, Xiaodong Long, Liang Bai, Xuerong Jia, Fengguo Zuo, Jie Tan, Yixin Guo, Peng Sun, Jun Zhou, Qiong Zhan, Sheng Hu, Yu Zhou, Yi Kang, Qiwei Ren, Xiping Jiang

Epitaxial Strain Control of $Hf_xZr_{1-X}O_2$ with Sub-Nm IGZO Seed Layer Achieving EOT=0.44 nm for DRAM Cell Capacitor 443
Seongho Kim, Young Keun Park, Gyu Soup Lee, Eui Joong Shin, Woon San Ko, Hi Deok Lee, Ga Won Lee, Byung Jin Cho

Highly Reliable and Manufacturable MRAM Embedded in 14nm FinFET Node 445
S. Ko, J. H. Park, J. H. Bak, H. Jung, J. Shim, D. S. Kim, W. Lim, D.-E. Jeong, J. H. Lee, K. Lee, J.-H. Park, Y. Kim, C. Kim, J. H. Jeong, C. Y. Lee, S. H. Han, Y. Ji, S. H. Hwang, H. J. Shin, K. Lee, Y. J. Song, Y. G. Shin, J. H. Song

U-MRAM: Transistor-Less, High-Speed (10 ns), Low-Voltage (0.6 V), Field-Free Unipolar MRAM for High-Density Data Memory 447
Ming-Hung Wu, Ming-Chun Hong, Ching Shih, Yao-Jen Chang, Yu-Chen Hsin, Shih-Ching Chiu, Kuan-Ming Chen, Yi-Hui Su, Chih-Yao Wang, Shan-Yi Yang, Guan-Long Chen, Hsin-Han Lee, Sk Ziaur Rahaman, I-Jung Wang, Chen-Yi Shih, Tsun-Chun Chang, Jeng-Hua Wei, Shyh-Shyuan Sheu, Wei-Chung Lo, Shih-Chieh Chang, Tuo-Hung Hou

Ongoing Evolution of DRAM Scaling via Third Dimension -Vertically Stacked DRAM - 449
J. W. Han, S. H. Park, M. Y. Jeong, K. S. Lee, K. N. Kim, H. J. Kim, J. C. Shin, S. M. Park, S. H. Shin, S. W. Park, K. S. Lee, J. H. Lee, S. H. Kim, B. C Kim, M. H. Jung, I. Y. Yoon, H. Kim, S. U. Jang, K. J. Park, Y. K. Kim, I. G. Kim, J. H Oh, S. Y. Han, B. S. Kim, B. J. Kuh, J. M. Park

Phase Change Memory-Based Hardware Accelerators for Deep Neural Networks (invited) 451
Geoffrey W. Burr, P. Narayanan, S. Ambrogio, A. Okazaki, H. Tsai, K. Hosokawa, C. Mackin, A. Nomura, T. Yasuda, J. Demarest, K. W. Brew, V. Chan, S. Choi, T. Gordon, T. M. Levin, A. Friz, M. Ishii, Y. Kohda, A. Chen, A. Fasoli, J. Luquin, N. Saulnier, S. Teehan, I. Ahsan, V. Narayanan

Non-Destructive-Read 1T1C Ferroelectric Capacitive Memory Cell with BEOL 3D Monolithically Integrated IGZO Access Transistor for $4F^2$ High-Density Integration 453
Zuopu Zhou, Leming Jiao, Qiwen Kong, Zijie Zheng, Kaizhen Han, Yue Chen, Chen Sun, Bich-Yen Nguyen, Xiao Gong

Foundry Monolithic 3D BEOL Transistor + Memory Stack: Iso-Performance and Iso-Footprint BEOL Carbon Nanotube FET+RRAM Vs. FEOL Silicon FET+RRAM 455
T. Srimani, A. C. Yu, R. M. Radway, D. T. Rich, M. Nelson, S. Wong, D. Murphy, S. Fuller, G. Hills, S. Mitra, M. M. Shulaker

Novel Cell Architectures with Back-Side Transistor Contacts for Scaling and Performance..... 457
M. Kobrinsky, J. D Silva, E. Mannebach, S. Mills, M. Abd El Qader, O. Adebayo, N. Arkali Radhakrishna, M. Beasley, J. Chawla, S. Chugh, A. Dasgupta, U. Desai, E. De Re, G. Dewey, T. Edwards, C. Engel, V. Gudmundsson, J. Hicks, B. Krist, R. Mehandru, I. Meric, P. Morrow, D. Nandi, P. Patel, R. Ramamurthy, D. Samanta, L. Shoer, A. St Amour, L. H. Tan, S. Yemenicioglu, X. Wang, T. Ghani

Nano-Through Silicon Vias (nTSV) for Backside Power Delivery Networks (BSPDN)..... 459
Eric Beyne, Anne Jourdain, Gerald Beyer

BEOL Interconnect Innovation: Materials, Process and Systems Co-Optimization for 3nm Node and Beyond..... 461
Gaurav Thareja, Ashish Pal, Xingye Wang, Sefa Dag, Shi You, Shashank Sharma, Qing Zhu, Carmen L. Cervantes, Shinjae Hwang, Matthew Spuller, Ben Ng, Pradeep S. Kumar, Norman Tam, Max Gage, Sameer Deshpande, Zhiyuan Wu, Alexander Jansen, Liton Dey, Feng Chen, Xianjin Xie, Keyvan Kashefizadeh, Vinod Reddy, Andy Lo, Zhebo Chen, Sidney Huey, Jianshe Tang, He Ren, Mehul Naik, Brian Brown, Sree Kesapragada, Buvna Ayyagari- Sangamali, El Mehdi Bazizi, Xianmin Tang

Block-Level Evaluation and Optimization of Backside PDN for High-Performance Computing at the A14 Node..... 463
G. Sisto, R. Preston, R. Chen, G. Mirabelli, A. Farokhnejad, Y. Zhou, I. Ciofi, A. Jourdain, A. Veloso, M. Stucchi, O. Zografos, P. Weckx, G. Hellings, J. Ryckaert

Structural Reliability and Performance Analysis of Backside PDN..... 465
Sunghwan Kim, Geun-Myeong Kim, Seong-Nam Kim, Saetbyeol Ahn, Yoon-Suk Kim, Inkook Jang, Kyoung-Woo Lee, Dae Sin Kim

Author Index