2023 IEEE International Memory Workshop (IMW 2023)

Monterey, California, USA
21 – 24 May 2023

IEEE Catalog Number:	**CFP23NOV-POD**
ISBN:	**978-1-6654-7460-3**

**Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP23NOV-POD
ISBN (Print-On-Demand):	978-1-6654-7460-3
ISBN (Online):	978-1-6654-7459-7
ISSN:	2330-7978

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

IMW 2023 TABLE OF CONTENTS

Schedule and Technical Program ix

Committee xi

Sponsors xiv

Session 1: Keynotes

[1.1] **28nm Data Memory with Embedded RRAM Technology in Automotive Microcontrollers** **1**
Alessandro Grossi, Matteo Coppetta, Stefano Aresu, Andreas Kux, Thomas Kern, and Robert Strenz

[1.2] **Recent Technology Insights on STT-MRAM: Structure, Materials, and Process Integration** **5**
Jeongdong Choe

[1.3] **Trends and Future Challenges of 3D NAND Flash Memory** **9**
Sun Il Shim, Jaehoon Jang, and Jaihyuk Song

Session 2: 3D NAND I

[2.1] **Improvement of GIDL-Assisted Erase by using Surrounded BL PAD Structure for VNAND** **13**
Suhwan Lim, Samki Kim, Changhee Lee, Hyeongwon Choi, Nambin Kim, Jaehun Jung, Hanvit Yang, Tae-Hun Kim, Junhee Lim, Daewon Ha, Sunghoi Hur, Jaehoon Jang, Yu-Gyun Shin, and Jaihyuk Song

[2.2] **Process Improvements for 7th Generation 1Tb Quad-Level Cell 3D NAND Flash Memory in Mass Production** **17**
Soochan Chung, Dong-Hyeon Ko, Joonsung Lim, Kyungmoon Kim, Sejie Takaki, Yujeong Seo, Byoungil Lee, Sejun Park, Jaeduk Lee, Kyungyoon Noh, Su Jin Ahn, and Sunghoi Hur

[2.3] **Distributed Cycling in Charge Trap-Based 3D NAND Arrays: Model and Qualification Tests Implications** **21**
Gianluca Nicosia, Niccolò Righetti, and Yingda Dong

Session 3: 3D DRAM & Selectors

[3.1] **A Simulation Study of Scaling Capability toward 10nm for the 3D Stackable Gate-Controlled Thyristor (GCT) DRAM Device** ***Invited*** **25**
Wei-Chen Chen, Hang-Ting Lue, Tzu-Hsuan Hsu, Keh-Chung Wang, and Chih-Yuan Lu

[3.2] **A 3D Stackable 1T1C DRAM: Architecture, Process Integration and Circuit Simulation** **29**
Meng Huang, Shufang Si, Zheng He, Ying Zhou, Sijia Li, Hong Wang, Jinying Liu, Dongsheng Xie, Mengmeng Yang, Kang You, Chris Choi, Yi Tang, Xiaojie Li, Shibing Qian, Xiaodong Yang, Long Hou, Weiping Bai, Zhongming Liu, Yanzhe Tang, Qiong Wu, Yanqin Wang, Tao Dou, Jake Kim, Gui-Lei Wang, Jie Bai, Adachi Takao, Chao Zhao, and Abraham Yoo

[3.3] Vertical Channel Transistor (VCT) as Access Transistor for Future $4F^2$ DRAM Architecture ***Late News*** 33
Daohuan Feng, Yi Jiang, Yunsong Qiu, Yuhong Zheng, Harry Kim, Jaewoo Kim, Jian Chu, Guangsu Shao, Yucheng Liao, Chen Yang, Minrui Hu, Wenli Zhao, Linjiang Xia, Jianfeng Xiao, Di Ma, Yuan Cheng, Xiangbo Kong, Chao Lin, Tianming Li, Yongjie Li, Jingheng Meng, Kai Shao, Yan Wang, Xiaoan Yang, Xiang Liu, Qinghua Han, Huiming Li, Yanzhe Tang, Mingde Liu, Eric Wu, Xiaoping Li, Renrui Huang, Mingtang Zhang, Long Hou, Xuan Pan, Xinwen Jin, Shuiping Zhao, DH Han, Ted Park, Deyuan Xiao, Chao Zhao, and Abraham Yoo

Posters Session

[P1] Analog Tuning of Floating-Gate Cells with Sub-Elementary Charge Accuracy for In-Memory Computing Applications ***Poster*** 37
Yuri Tkachev, Steven Lemke, Louisa Schneider, Gilles Festes, and Parviz Ghazavi

[P2] Comprehensive Study of Endurance Fatigue in the Scaled Si FeFET by In-Situ V_{th} Measurement and Endurance Enhancement Strategy ***Poster*** 41
Xianzhou Shao, Junshuai Chai, Min Liao, Jiahui Duan, Fengbin Tian, Xiaoyu Ke, Xiaoqing Sun, Hao Xu, Jinjuan Xiang, Xiaolei Wang, and Wenwu Wang

[P3] 7-Bit/2Cell (X3.5), 9-Bit/2Cell (X4.5) NAND Flash Memory: Half Bit Technology ***Poster*** 45
Noboru Shibata, Hironori Uchikawa, Taira Shibuya, Kenri Nakai, Kosuke Yanagidaira, and Hirofumi Inoue

[P4] Eliminating Capacitive Sneak Paths in Associative Capacitive Networks Based on Complementary Resistive Switches for In-Memory Computing ***Poster*** 49
Tobias Ziegler, Leon Brackmann, Tyler Hennen, Christopher Bengel, Stephan Menzel, and Dirk J. Wouters

[P5] Demonstration of SMT-Reflow Immune and SCA-Resilient PUF on 28nm RRAM Device Array ***Poster*** 53
Vivek Parmar, Sandeep Kaur Kingra, Deepak Verma, Digamber Pandey, Giuseppe Piccolboni, Alessandro Bricalli, Amir Regev, Gabriel Pares, Laurent Grenouillet, Jean-François Nodin, and Manan Suri

[P6] Design of Ferroelectric-Metal Field-Effect Transistor for Multi-Level-Cell 3D NAND Flash ***Poster*** 57
Sola Woo, Gihun Choe, Asif Islam Khan, Suman Datta, and Shimeng Yu

[P7] A Comprehensive Study on the Pillar Size of OTS-PCM Memory with an Optimized Process and Scaling Trends Down to Sub-10 nm for SCM Applications ***Poster*** 61
W.C. Chien, E.K. Lai, L. Buzi, C.W. Cheng, C.W. Yeh, A. Ray, L.M. Gignac, N. Gong, H.Y. Cheng, A. Grun, D.Y. Lee, W. Kim, A. Majumdar, D. Bishop, R.L. Bruce, D. Daudelin, H.Y. Ho, M. BrightSky, and H.L. Lung

[P8] Effect of High-Temperature Bake on RTN Statistics in Floating Gate Flash Memory Arrays ***Poster*** 65
Viktor Markov, Gilles Festes, Louisa Schneider, Steven Lemke, Serguei Jourba, and Alexander Kotov

[P9] Dielectric Relaxation Performance of DRAM Storage Capacitors and Ways of Improvement ***Poster*** 69
Z. Asher Bai, Yixian Wang, Lixue Liu, Xi Zhang, Feng Yuan, Junsheng Meng, Zhongming Liu, JS Jeon, James Cho, Blacksmith Wu, Huihui Li, Guilei Wang, Chao Zhao, and Kanyu Cao

[P10] In-Memory Neural Network Accelerator Based on Phase Change Memory (PCM) with One-Selector/One-Resistor (1S1R) Structure Operated in the Subthreshold Regime ***Poster*** 73
N. Lepri, P. Gibertini, P. Mannocci, A. Pirovano, I. Tortorelli, P. Fantini, and D. Ielmini

[P11] Benefits of Design Assist Techniques on Performances and Reliability of a RRAM Macro ***Poster*** 77
B. Giraud, S. Ricavy, Y. Moursy, C. Laffond, I. Sever, V. Gherman, M. Pezzin, F. Lepin, M. Diallo, K. Zenati, S. Dumas, M. Vershkov, A. Bricalli, G. Piccolboni, J.-P. Noel, A. Samir, G. Pillonnet, Y. Thonnart, and G. Molas

[P12] SONOS Embedded Flash IP using Trap-Depth-Controlled SiN Film Enabling Data Retention more than 10 years at 200°C ***Poster*** 81
Yasuhiro Taniguchi, Shoji Yoshida, Teruhiko Egashira, ChihBin Kuo, YiYang Shie, YuChun Wang, ChenYu Huang, Tsuyoshi Tamatsu, Keiji Okamoto, Masanobu Hishiki, Yasushi Sasaki, Fukuo Owada, Nobuhiko Ito, Yutaka Shinagawa, ChihMing Kuo, Satoshi Noda, Toshikazu Matsui, and Kosuke Okuyama

[P13] Stochastic Computing-Based Computation-in-Memory (SC CiM) Architecture for DNNs and Hierarchical Evaluations of Non-Volatile Memory Error and Defect Tolerance ***Poster*** 85
Takuto Nishimura, Yuya Ichikawa, Akira Goda, Naoko Misawa, Chihiro Matsui, and Ken Takeuchi

[P14] Ferroelectric HfO_2/ZrO_2 Superlattices with Improved Leakage at Bias and Temperature Stress ***Poster*** 89
David Lehninger, Ayse Sünbül, Ricardo Olivo, Thomas Kämpfe, Konrad Seidel, and Maximilian Lederer

Session 4: Ferro

[4.1] Hafnium Oxide-Based Ferroelectric Memories: Are We Ready for Application? ***Invited*** 93
Konrad Seidel, David Lehninger, Franz Müller, Yannick Raffel, Ayse Sünbül, Ricardo Revello, Raik Hoffmann, Sourav De, Thomas Kämpfe, and Maximilian Lederer

[4.2] Improved MW of IGZO-Channel FeFET by Reading Scheme Optimization and Interfacial Engineering 97
Zhuo Chen, Nicolo Ronchi, Amey Walke, Kaustuv Banerjee, Mihaela Ioana Popovici, Kostantine Katcko, Geert Van den bosch, Maarten Rosmeulen, Valeri Afanas'ev, and Jan Van Houdt

[4.3] Memory Window in Si:HfO_2 FeRAM arrays: Performance Improvement and Extrapolation at Advanced Nodes 101
J. Laguerre, M. Bocquet, O. Billoint, S. Martin, J. Coignus, C. Carabasse, T. Magis, T. Dewolf, F. Andrieu, and L. Grenouillet

[4.4] Optimization of Retention in Ferroelectricity Boosted Gate Stacks for 3D NAND 105
L. Breuil, M. Popovici, J. Stiers, A. Arreghini, S. Ramesh, G. Van den bosch, J. Van Houdt, and M. Rosmeulen

Session 5: 3D NAND II

[5.1] Towards Improving Ionizing Radiation Tolerance of 3-D NAND Flash Memory ***Invited*** **109**
Biswajit Ray, Matchima Buddhanoy, and Mondol Anik Kumar

[5.2] Physical Model and Characteristics of 3D NAND Memory Cell Metastability Issues under High Temperature Stress **113**
Andrew Bicksler, Carmine Miccoli, and Srinath Venkatesan

[5.3] Proposal of P-Channel FE NAND with High Drain Current and Feasible Disturbance for Next Generation 3D NAND **117**
Song-Hyeon Kuk, Jae-Hoon Han, Bong Ho Kim, Junpyo Kim, and Sang-Hyeon Kim

[5.4] Enabling 3D NAND Trench Cells for Scaled Flash Memories **121**
S. Rachidi, S. Ramesh, L. Breuil, Z. Tao, D. Verreck, G. L. Donadio, A. Arreghini,
G. Van den bosch, and M. Rosmeulen

Session 6: Systems, STT & RRAM

[6.1] An 18nm ePCM with BJT Selector NVM Design for Advanced Microcontroller Applications ***Invited*** **125**
Antonino Conte, Francesco Tomaiuolo, Marco Ruta, Andrea Redaelli, Franck Arnaud,
Thomas Jouanneau, Christian Boccaccio, and Olivier Weber

[6.2] Low Power and Thermal Throttling-Less SSD with In-Package Boost Converter for 1000-WL Layer 3D Flash Memory **129**
Kazuma Hasegawa, Yuta Aiba, Xu Li, Hitomi Tanaka, Takayuki Miyazaki, Hideko Mukaida,
Masaru Koyanagi, Masayuki Miura, and Tomoya Sanuki

[6.3] Voltage Control of Magnetism: Low-Power Spintronics ***Invited*** **133**
Astha Khandelwal, Rajesh Chopdekar, Akash Surampalli, Kaushal Tiwari, Naveen Negi,
Alan Kalitsov, Lei Wan, Jordan Katine, Derek Stewart, Tiffany Santos, Yen-Lin Huang,
R. Ramesh, and Bhagwati Prasad

[6.4] Physical Modeling and Design Rules of Analog Conductive Metal Oxide-HfO_2 ReRAM **137**
Donato Francesco Falcone, Stephan Menzel, Tommaso Stecconi, Antonio La Porta,
Ludovico Carraria-Martinotti, Bert Jan Offrein, and Valeria Bragaglia

Session 7: Neuromorphic/In-Mem

[7.1] Spin-Orbit Torque MRAM for Ultrafast Cache and Neuromorphic Computing Applications ***Invited*** **141**
Siddharth Rao, Kaiming Cai, Giacomo Talmelli, Nathali Franchina-Vergel, Ward Janssens,
Hubert Hody, Farrukh Yasin, Kurt Wostyn, and Sebastien Couet

[7.2] SLC and MLC In-Memory-Approximate-Search Solutions in Commercial 48-Layer and 96-Layer 3D-NAND Flash Memories **145**
Po-Hao Tseng, Tian-Cig Bo, Yu-Hsuan Lin, Yu-Chao Lin, Jhe-Yi Liao, Feng-Ming Lee,
Yu-Yu Lin, Ming-Hsiu Lee, Kuang-Yeu Hsieh, Keh-Chung Wang, and Chih-Yuan Lu

[7.3] Multi-Level Operation of Ferroelectric FET Memory Arrays for Compute-In-Memory Applications **149**
Franz Müller, Sourav De, Maximilian Lederer, Raik Hoffmann, Ricardo Olivo, Thomas Kämpfe, Konrad Seidel, Tarek Ali, Halid Mulaosmanovic, Stefan Dünkel, Johannes Müller, Sven Beyer, and Gerald Gerlach

[7.4] Demonstration of Multilevel Multiply Accumulate Operations for AiMC using Engineered a-IGZO Transistors-Based 2T1C Gain Cell Arrays **153**
Subhali Subhechha, Stefan Cosemans, Attilio Belmonte, Nouredine Rassoul, Shamin Houshmand Sharifi, Peter Debacker, Diederik Verkest, Romain Delhougne, and Gouri Sankar Kar

Session 8: 3D Processing

[8.1] Materials Enabled Memory Scaling and New Architectures ***Invited*** **157**
Zhijun Chen, Fred Fishburn, Chang Seok Kang, Sony Varghese, and Bala Haran

[8.2] Overlay Control in HAR Device Integration **161**
Pradeep Subrahmanyan, Wonjae Lee, Jeff Lischer, Ram Karur, Olga Kucher, Stan Todorov, and Adaeze Osonkie

Author Index **165**