

# **2023 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2023)**

**Tallinn, Estonia  
3 – 5 May 2023**



**IEEE Catalog Number: CFP23DDE-POD  
ISBN: 979-8-3503-3278-0**

**Copyright © 2023 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP23DDE-POD
ISBN (Print-On-Demand):	979-8-3503-3278-0
ISBN (Online):	979-8-3503-3277-3
ISSN:	2334-3133

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## TABLE OF CONTENTS

Evaluating the Hardware Performance Counters of an Xtensa Virtual Prototype .....	1
<i>Adebayo Omotosho, Sirine Ilahi, Ernesto Cristopher Villegas Castillo, Christian Hammer, Christian Sauer</i>	
Optimizing Packet Classification on FPGA .....	7
<i>Michal Kekely, Jan Korenek</i>	
Active Wire Fences for Multitenant FPGAs.....	13
<i>Ognjen Glamocanin, Andela Kostic, Staša Kostic, Mirjana Stojilovic</i>	
Collecting Diagnostic Information Through Dichotomic Search from Logic BIST of Failing In-Field Automotive SoCs with Delay Faults .....	21
<i>Paolo Bernardi, Gabriele Filippini, Matteo Sonza Reorda, Davide Appello, Claudia Bertani, Vincenzo Tancorre</i>	
Data-Driven Test Generation for Black-Box Systems from Learned Decision Tree Models .....	27
<i>Swantje Plambeck, Goerschwin Fey</i>	
Reducing Output Response Aliasing Using Boolean Optimization Techniques.....	33
<i>Robert Hülle, Petr Fišer, Jan Schmidt</i>	
Split-Et-Impera: A Framework for the Design of Distributed Deep Learning Applications.....	39
<i>Luigi Capogrosso, Federico Cunico, Michele Lora, Marco Cristani, Franco Fummi, Davide Quaglia</i>	
Prediction of Inference Energy on CNN Accelerators Supporting Approximate Circuits.....	45
<i>Michal Pinos, Vojtech Mrazek, Lukas Sekanina</i>	
NeuroPIM: Flexible Neural Accelerator for Processing-in-Memory Architectures .....	51
<i>Ali Monavari Bidgoli, Sepideh Fattahi, Seyyed Hossein Seyyedaghaei Rezaei, Mehdi Modarressi, Masoud Daneshlab</i>	
Hardware Acceleration of FHEW.....	57
<i>Jonas Bertels, Michiel Van Beirendonck, Furkan Turan, Ingrid Verbauwhede</i>	
Supporting Analog Design for Reliability by Efficient Provision of Reliability Information to Designers.....	61
<i>Fabio A. Velarde Gonzalez, Lukas Hahne, Katrin Ortstein, André Lange, Sonja Crocoll</i>	
Characterization of Interconnect Fault Effects in SRAM-Based FPGAs .....	65
<i>Christian Fibich, Martin Horauer, Roman Obermaisser</i>	
LUTIC: A CRAM-Based Architecture for Power Failure Resilient In-Memory Computing .....	69
<i>Khakim Akhunov, Kasim Sinan Yildirim</i>	
Efficient Binary Decision Diagram Manipulation by Reducing the Number of Intermediate Nodes .....	73
<i>Rune Krauss, Mehran Goli, Rolf Drechsler</i>	
High-Throughput Approximate Multiplication Models in PyTorch.....	79
<i>Elias Trommer, Bernd Waschneck, Akash Kumar</i>	
A Low-Cost Residue-Based Scheme for Error-Resiliency of RNN Accelerators .....	83
<i>Nooshin Nosrati, Zainalabedin Navabi</i>	

HermesBDD: A Multi-Core and Multi-Platform Binary Decision Diagram Package .....	87
<i>Luigi Capogrosso, Luca Geretti, Marco Cristani, Franco Fummi, Tiziano Villa</i>	
Approximation of Hardware Accelerators Driven by Machine-Learning Models: (Embedded Tutorial) .....	91
<i>Vojtech Mrazek</i>	
Structured Design and Evaluation of a Resistor-Based PUF Robust Against PVT-Variations .....	93
<i>Carl Riehm, Christoph Frisch, Florin Burcea, Matthias Hiller, Michael Pehl, Ralf Brederlow</i>	
Counterfeit Chip Detection Using Scattering Parameter Analysis .....	99
<i>Maryam Saadat Safa, Tahoura Mosavirik, Shahin Tajik</i>	
Quality Assessment of Logic Locking Mechanisms Using Pseudo-Boolean Optimization Techniques .....	105
<i>Marcel Merten, Muhammad Hassan, Rolf Drechsler</i>	
A Digital Delay Model Supporting Large Adversarial Delay Variations .....	111
<i>Daniel Öhlinger, Ulrich Schmid</i>	
A Lightweight Intrusion Detection System Against IoT Memory Corruption Attacks .....	118
<i>Mohamed El Bouazzati, Russell Tessier, Philippe Tanguy, Guy Gogniat</i>	
APPRAISER: DNN Fault Resilience Analysis Employing Approximation Errors .....	124
<i>Mahdi Taheri, Mohammad Hasan Ahmadilivani, Maksim Jenihhin, Masoud Daneshtalab, Jaan Raik</i>	
A Configurable Mixed-Precision Convolution Processing Unit Generator in Chisel .....	128
<i>Jure Vreca, Anton Biasizzo</i>	
Open Automation Framework for Complex Parametric Electrical Simulations .....	132
<i>Sergio Vinagrero Gutiérrez, Pietro Inglese, Giorgio Di Natale, Elena-Ioana Vatajelu</i>	
A Low-Cost Combinational Approximate Multiplier .....	136
<i>Zahra Hojati, Zainalabedin Navabi</i>	
Bits, Flips and RISCs .....	140
<i>Nicolas Gerlin, Endri Kaja, Fabian Vargas, Li Lu, Anselm Breitenreiter, Junchao Chen, Markus Ulbricht, Maribel Gomez, Ares Tahiraga, Sebastian Prebeck, Eyck Jentzsch, Miloš Krstic, Wolfgang Ecker</i>	
Standalone Area Optimized ASIC Tag Powered and Programmable by Light for Identification of Novel Drug Candidates .....	150
<i>Dominic Korner, Andreas Kramer, Klaus Hofmann, Felix Hausch</i>	
MODEE-LID: Multiobjective Design of Energy-Efficient Hardware Accelerators for Levodopa-Induced Dyskinesia Classifiers .....	155
<i>Martin Hurta, Vojtech Mrazek, Michaela Drahosova, Lukas Sekanina</i>	
Verifying Bio-Electronic Systems .....	161
<i>Joseline Heuer, René Krenz-Bääth, Roman Obermaisser</i>	
Embedded Tutorial - RRAMs: How to Guarantee Their Quality Test After Manufacturing? .....	167
<i>L. M. Bolzani Poehls</i>	

A Reliability-Aware Environment for Design Exploration for GPU Devices .....	169
<i>Robert Limas Sierra, Juan-David Guerrero-Balaguera, Josie E. Rodriguez Condia, Matteo Sonza Reorda</i>	
A Comprehensive Analysis of Transient Errors on Systolic Arrays .....	175
<i>Eleonora Vacca, Sarah Azimi, Luca Sterpone</i>	
Resilience-Performance Tradeoff Analysis of a Deep Neural Network Accelerator .....	181
<i>Salvatore Pappalardo, Annachiara Ruospo, Ian O'Connor, Bastien Deveautour, Ernesto Sanchez, Alberto Bosio</i>	

**Author Index**