2022 IEEE 40th International Conference on Computer Design (ICCD 2022)

Olympic Valley, California, USA 23 – 26 October 2022



IEEE Catalog Number: CFP22ICD-POD **ISBN:**

978-1-6654-6187-0

Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:	
ISBN (Print-On-Demand):	
ISBN (Online):	
ISSN:	

CFP22ICD-POD 978-1-6654-6187-0 978-1-6654-6186-3 1063-6404

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400 Fax: (845) 758-2633 E-mail: curran@proceedings.com Web: www.proceedings.com



2022 IEEE 40th International Conference on Computer Design (ICCD) ICCD 2022

Table of Contents

Message from the General Chair	xxi
Message from the Program Chairs	xxii
Organizing Committee	xxiii
Program Committee	xxiv
External Reviewers	xxviii
Keynotes	xxix
Sponsors	xxxii
External Reviewers	xxiv xxviii xxix xxix xxix

Session 1A: Circuit Design

A Flash-Based Digital to Analog Converter for Low Power Applications
Accurate Prediction of ReRAM Crossbar Performance Under I-V Nonlinearity and IR Drop
RHSCC-16T: Radiation Hardened Sextuple Cross Coupled Robust SRAM Design for Radiation Prone Environments

Session 1B: Memory Architectures

Supporting Dynamic Translation Granularity for Hybrid Memory Systems	
Bokyeong Kim (Samsung Research), Soojin Hwang (KAIST), Sanghoon Cha	
(Samsung Advanced Institute of Technology), Chang Hyun Park (Uppsala	
University), Jongse Park (KAIST), and Jaehyuk Huh (KAIST)	

 HyFarM: Task Orchestration on Hybrid Far Memory for High Performance Per Bit
 Reexamining CGRA Memory Sub-System for Higher Memory Utilization and Performance

Session 2A: Caches and Disks

SLAP-CC: Set-Level Adaptive Prefetching for Compressed Caches Laith Albarakat (Texas A&M University, USA), Paul V. Gratz (Texas A&M University, USA), and Daniel A. Jiménez (Texas A&M University, USA)	50
PACA: A Page Type Aware Read Cache Scheme in QLC Flash-Based SSDs Qihui Chen (Huazhong University of Science and Technology, China), Shuai Wang (Alibaba Group, China), You Zhou (Huazhong University of Science and Technology, China), Fei Wu (Huazhong University of Science and Technology, China), Shu Li (Alibaba Group, China), Zhengyong Wang (Alibaba Group, China), and Changsheng Xie (Huazhong University of Science and Technology, China)	59
A Multi-Factor Adaptive Multi-Level Cooperative Replacement Policy in Block Storage Systems	67
Contention Tracking in GPU Last-Level Cache Javier Barrera (Barcelona Supercomputing Center, Spain; Universitat Politecnica de Barcelona, Spain), Leonidas Kosmidis (Barcelona Supercomputing Center, Spain; Universitat Politecnica de Barcelona, Spain), Hamid Tabani (Barcelona Supercomputing Center, Spain), Jaume Abella (Barcelona Supercomputing Center, Spain), and Francisco J. Cazorla (Barcelona Supercomputing Center, Spain)	76

Session 2B: Secure Systems

 Secure Access Policy (SAP): Invisibly Executing Speculative Unsafe Accesses in an Isolated Environment	0
DNNCloak: Secure DNN Models Against Memory Side-Channel Based Reverse Engineering Attacks	9
MultiCon: An Efficient Timing-Based Side Channel Attack on Shared Memory Multicores	7
Tunable Memory Protection for Secure Neural Processing Units	5

Session 3A: Noise-Aware Quantum Synthesis and Compilation (Special Session)

Design and Analysis of a Scalable and Efficient Quantum Circuit for LWE Matrix Arithmetic 109 Chao Lu (University of Texas at Dallas, USA), Utsav Banerjee (Indian Institute of Science, India), and Kanad Basu (University of Texas, USA))
Optimization of Quantum Read-Only Memory Circuits	,
 Exploiting Quantum Assertions for Error Mitigation and Quantum Program Debugging	:
Modeling of Noisy Quantum Circuits Using Random Matrix Theory	-
Machine Learning for Quantum Hardware Performance Assessment)

Session 3B: Architectures and Systems

 Enhancing GPU Performance via Neighboring Directory Table Based Inter-TLB Sharing
 GRPU: An Efficient Graph-Based Cross-Rack Parallel Update Scheme for Cloud Storage Systems 154 Ranhao Jia (Shanghai Jiao Tong University, China), Haiwei Deng (Shanghai Jiao Tong University, China), Yunfei Gu (Shanghai Jiao Tong University, China), Huangzhen Xue (Shanghai Jiao Tong University, China), Chentao Wu (Shanghai Jiao Tong University, China), Shiyi Li (Harbin Institute of Technology, Shenzhen, China), Jie Li (Shanghai Jiao Tong University, China), Guangtao Xue (Shanghai Jiao Tong University, China), and Minyi Guo (Shanghai Jiao Tong University, China)
 Accelerating Garbage Collection of 3D Flash Memory via Exploiting Inter-Channel Parallelism
 SuperCDC: A Hybrid Design of High-Performance Content-Defined Chunking for Fast Deduplication
HaLSM: A Hotspot-Aware LSM-Tree Based Key-Value Storage Engine

Session 4A: Computing System Design

Adaptive Size-Aware Cache Insertion Policy for Content Delivery Networks	195
Peng Wang (Huazhong University of Science and Technology, China), Yu	
Liu (Huazhong University of Science and Technology, China), Zhelong	
Zhao (Huazhong University of Science and Technology, China), Ke Zhou	
(Huazhong University of Science and Technology, China), Zhihai Huang	
(Tencent Technology (Shenzhen) Co., Ltd., China), and Yanxiong Chen	
(Tencent Technology (Shenzhen) Co., Ltd., China)	
Scheduling Information-Guided Efficient High-Level Synthesis Design Space Exploration	203
Xingyue Qian (University of Michigan-SJTU Joint Institute), Jian Shi	
(University of Michigan-SJTU Joint Institute), Li Shi (University of	
Michigan-SJTU Joint Institute), Haoyang Zhang (University of	
Michigan-SJTU Joint Institute), Lijian Bian (Shanghai AnLogic Infotech	
Co., Ltd, China), and Weikang Qian (University of Michigan-SJTU Joint	
Institute; Shanghai Jiao Tong University, China)	

Session 4B: Machine Learning, EDA, and Heterogeneous Computing: How the Trio Pave the Future (Special Session)

AI-Assisted Synthesis in Next Generation EDA: Promises, Challenges, and Prospects
Auto-Tuning of AI/ML Graphs for Optimal Performance in a Heterogenous Processor System 215 Ravikumar V Chakaravarthy (AMD Inc., USA), Hua Jiang (AMD Inc., USA), Raghav Chakravarthy (Centennial High School, USA), and Siddharth Das (Georgia Institute of Technology, USA)
Optimizing ML Classification Models for Constrained EDA Resource Budgets

Session 5A: Security and Reliability

Sridhar Rajakumar (Synopsys Inc)

Breakthrough to Adaptive and Cost-Aware Hardware-Assisted Zero-Day Malware Detection: A Reinforcement Learning-Based Approach Zhangying He (California State University, USA), Hosein Mohammadi Makrani (University of California, USA), Setareh Rafatirad (University of California, USA), Houman Homayoun (University of California, USA), and Hossein Sayadi (California State University, USA)	231
A Black-Box Sensitization Attack on SAT-Hard Instances in Logic Obfuscation Isaac Mcdaniel (University of Maryland, USA), Michael Zuzak (Rochester Institute of Technology, USA), and Ankur Srivastava (University of Maryland, USA)	239
Efficient Finite State Machine Encoding for Defending Against Laser Fault Injection Attacks Aruna Jayasena (University of Florida, USA), Khushboo Rani (University of Florida, USA), and Prabhat Mishra (University of Florida, USA)	247

 Analysis and Mitigation of Data Sanitization Overhead in DAX File Systems
Iron-Dome: Securing IoT Networked Systems at Runtime by Network and Device Characteristics to Confine Malware Epidemics
Session 5B: Algorithm–Hardware Co-Design for Graph Neural Networks (Special Session)
 Towards Real-Time Temporal Graph Learning
 Towards Sparsification of Graph Neural Networks
CoDG-ReRAM: An Algorithm-Hardware Co-Design to Accelerate Semi-Structured GNNs on ReRAM
Yixuan Luo (University of Rochester), Payman Behnam (Georgia Institute of Technology), Kiran Thorat (University of Connecticut), Zhuo Liu (University of Rochester), Hongwu Peng (University of Connecticut), Shaoyi Huang (University of Connecticut), Shu Zhou (University of Rochester), Omer Khan (University of Connecticut), Alexey Tumanov (Georgia Institute of Technology), Caiwen Ding (University of Connecticut), and Tong Geng (University of Rochester)
On the Design of Quantum Graph Convolutional Neural Network in the NISQ-Era and Beyond 290 Zhirui Hu (George Mason University), Jinyang Li (George Mason University), Zhenyu Pan (University of Rochester), Shanglin Zhou (University of Connecticut), Lei Yang (George Mason University), Caiwen Ding (University of Connecticut), Omer Khan (University of Connecticut), Tong Geng (University of Rochester), and Weiwen Jiang

(George Mason University)

Session 6A: Disks and File Systems

 ES4D: Accelerating Exact Similarity Search for High-Dimensional Vectors via Vector Slicing and In-SSD Computation	18
InDeF: An Advanced Defragmenter Supporting Migration Offloading on ZNS SSD	17
 A Focused Garbage Collection Approach for Primary Deduplicated Storage with Low Memory Overhead	.5
 DPLFS: A Dual-Mode PCM-Based Log-Structured File System	:4
Log-ROC: Log Structured RAID on Open-Channel SSD	2

Session 6B: Novel Architectures

CPR: Crossbar-Grain Pruning for an RRAM-Based Accelerator with Coordinate-Based Weight Mapping Jihye Park (Pohang University of Science and Technology, South Korea) and Seokhyeong Kang (Pohang University of Science and Technology, South Korea)	. 336
SoftFusion: A Low-Cost Approach to Enhance Reliability of Object Detection Applications Salar Latifi (University of Michigan, USA), Babak Zamirai (University of Michigan, USA), and Scott Mahlke (University of Michigan, USA)	344
Cost-Aware TVM (CAT) Tensorization for Modern Deep Learning Accelerators Yahang Hu (National University of Defense Technology), Yaohua Wang (National University of Defense Technology), Xiaoqiang Dan (Stream Computing Inc.), Xiao Hu (National University of Defense Technology), Fei Liu (Stream Computing Inc.), and Jinpeng Li (Stream Computing Inc.)	. 352

Segmenting Age Matrices to Improve Instruction Scheduling Without Increasing Delay and Area
 AOME: Autonomous Optimal Mapping Exploration Using Reinforcement Learning for NoC-Based Accelerators Running Neural Networks
VSA: A Hybrid Vector-Systolic Architecture
CNN Acceleration with Joint Optimization of Practical PIM and GPU on Embedded Devices 372 Tianyu Wang (The Chinese University of Hong Kong, China), Zhaoyan Shen (Shandong University, China), and Zili Shao (The Chinese University of Hong Kong, China)

Purlin: A Versatile Toolkit for the Generation and Simulation of On-Chip Network	85
Yijiang Guo (Peking University), Xinming Wei (Peking University),	
Jiaxi Zhang (Peking University; Peng Cheng Laboratory), and Guojie Luo	
(Peking University; Peng Cheng Laboratory)	
Hardware Minimization of Two-Level Adiabatic Logic Based on Weighted Maximum Stable Set	

Session 7B: Computer Systems

A Lightweight and Adaptive Cache Partitioning Scheme for Content Delivery Networks
 ZNSKV: Reducing Data Migration in LSMT-Based KV Stores on ZNS SSDs
 BP-Im2col: Implicit Im2col Supporting AI Backpropagation on Systolic Arrays

Session 8A: AI Architectures

Do Not Forget: Exploiting Stability-Plasticity Dilemma to Expedite Unsupervised SNN Training for Neuromorphic Processors Myeongjin Kwak (Kyungpook National University, Republic of Korea) and Yongtae Kim (Kyungpook National University, Republic of Korea)	419
Accelerating the Training of Single Layer Binary Neural Networks Using the HHL Quantum Algorithm Sonia Lopez Alarcon (Rochester Institute of Technology, USA), Cory	427
Merkel (Rochester Institute of Technology, USA), Martin Hoffnagle (Rochester Institute of Technology, USA), Sabrina Ly (Rochester Institute of Technology, USA), and Alejandro Pozas-Kerstjens (Institute of Mathematical Sciences (CSIC-UCM-UC3M-UAM), Spain)	
HL-DNA: A Hybrid Lossy/Lossless Encoding Scheme to Enhance DNA Storage Density and Robustness for Images Yi Li (Oklahoma State University, USA), David Du (University of Minnesota, Twin Cities, USA), Li Ou (University of Minnesota, Twin Cities, USA), and Bingzhe Li (Oklahoma State University, USA)	434
LightNorm: Area and Energy-Efficient Batch Normalization Hardware for On-Device DNN Training Seock-Hwan Noh (DGIST, South Korea), Junsang Park (DGIST, South Korea), Dahoon Park (DGIST, South Korea), Jahyun Koo (DGIST, South Korea), Jeik Choi (DGIST, South Korea), and Jaeha Kung (DGIST, South Korea)	443

Randomize and Match: Exploiting Irregular Sparsity for Energy Efficient Processing in SNNs....... 451 Fangxin Liu (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute), Zongwu Wang (Shanghai Jiao Tong University), Wenbo Zhao (Shanghai Jiao Tong University), Yongbiao Chen (Shanghai Jiao Tong University), Tao Yang (Shanghai Jiao Tong University), Xiaokang Yang (Shanghai Jiao Tong University), and Li Jiang (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute)

Session 8B: Processor Architectures I

Instruction-Aware Learning-Based Timing Error Models Through Significance-Driven Approximations
[*] Styliani Tompazi (Queen's University Belfast, UK), Ioannis Tsiokanos (Queen's University Belfast, UK; Athens Research & Development Center, U-blox), Jesus Martinez Del Rincon (Queen's University Belfast, UK), Lev Mukhanov (Queen's University Belfast, UK), and Georgios Karakonstantis (Queen's University Belfast, UK)
In-Depth Testing of x86 Instruction Disassemblers with Feedback Controlled DFS Algorithm 463 Guang Wang (Institute of Information Engineering, CAS; University of Chinese Academy of Sciences), Ziyuan Zhu (Institute of Information Engineering, CAS; University of Chinese Academy of Sciences), Xu Cheng (Peking University), and Dan Meng (Institute of Information Engineering, CAS; University of Chinese Academy of Sciences)
 Composite Instruction Prefetching
 Sparkle: A High Efficient Sparse Matrix Multiplication Accelerator for Deep Learning
FHAM: FPGA-Based High-Efficiency Approximate Multipliers via LUT Encoding

Session 9A: AI Systems

LEAPER: Fast and Accurate FPGA-Based System Performance Prediction via Transfer Learning 499 Gagandeep Singh (ETH Zurich), Dionysios Diamantopoulos (IBM Research Europe, Zurich), Juan Gómez-Luna (ETH Zurich), Sander Stuijk (Eindhoven University of Technology), Henk Corporaal (Eindhoven University of Technology), and Onur Mutlu (ETH Zurich)
 VEA: An FPGA-Based Voxel Encoding Accelerator for 3D Object Detection with LiDAR
 Full Stack Parallel Online Hyperdimensional Regression on FPGA
HPMA-Saber: High-Performance Polynomial Multiplication Accelerator for KEM Saber

Session 9B: Processor Architectures II

A Highly-Efficient Error Detection Technique for General Matrix Multiplication Using Tiled Processing on SIMD Architecture Chandra Sekhar Mummidi (University of Massachusetts, USA), Sandeep Bal (University of Massachusetts, USA), Brunno F. Goldstein (Universidade Federal do Rio de Janeiro, Brazil), Sudarshan Srinivasan (Intel Labs, India), and Sandip Kundu (University of Massachusetts, USA)	529
 Fault Localization for Hardware Design Code with Time-Aware Program Spectrum	537
FSA: An Efficient Fault-Tolerant Systolic Array-Based DNN Accelerator Architecture Yingnan Zhao (George Washington University), Ke Wang (University of North Carolina at Charlotte), and Ahmed Louri (George Washington University)	545
RelHD: A Graph-Based Learning on FeFET with Hyperdimensional Computing Jaeyoung Kang (University of California San Diego, USA), Minxuan Zhou (University of California San Diego, USA), Abhinav Bhansali (University of California San Diego, USA), Weihong Xu (University of California San Diego, USA), Anthony Thomas (University of California San Diego, USA), and Tajana Rosing (University of California San Diego, USA)	553

NeuroFabric: Hardware and ML Model Co-Design for A Priori Sparse Neural Network Training .. 561 Mihailo Isakov (Arizona State University) and Michel A. Kinsy (Arizona State University)

Session 10A: Hardware Security and Trust (Special Session)

Area Efficient Asynchronous Circuits for Side Channel Attack Mitigation Dallas Phillips (University of Cincinnati, USA), Pingxiuqi Chen (University of Cincinnati, USA), and John Emmert (University of Cincinnati, USA)	565
Transition Recovery Attack on Embedded State Machines Using Power Analysis Clay Carper (University of Wyoming, USA), Andey Robins (University of Wyoming, USA), and Mike Borowczak (University of Wyoming, USA)	572
Trojan Resilience in Implantable and Wearable Medical Devices with Virtual Biosensing Shakil Mahmud (University of South Florida, USA), Farhath Zareen (University of South Florida, USA), Brooks Olney (University of South Florida, USA), Mateus A. Fernandes A. (University of South Florida, USA), and Robert Karam (University of South Florida, USA)	577
Model Checking Leveraged Error Localization for Complex RTL Designs	585

Session 10B: Data Management

 NapFS: A High-Performance NUMA-Aware PM File System	593
SoftSSD: Software-Defined SSD Development Platform for Rapid Flash Firmware Prototyping 6 Jin Xue (The Chinese University of Hong Kong, China), Renhai Chen (Tianjin University, China), and Zili Shao (The Chinese University of Hong Kong, China)	502
 Tripod: Harmonizing Job Scheduling and Data Caching for Analytics Frameworks	510

FedNorm: An Efficient Federated Learning Framework with Dual Heterogeneity Coexistence on Edge Intelligence Systems
Zirui Lian (University of Science and Technology of China, China), Weihong Liu (University of Science and Technology of China, China), Jing Cao (University of Science and Technology of China, China), Zongwei Zhu (University of Science and Technology of China, China), and Xuehai Zhou (University of Science and Technology of China, China)
Session 11A: Neural Networks
 Collate: Collaborative Neural Network Learning for Latency-Critical Edge Systems
TermiNETor: Early Convolution Termination for Efficient Deep Neural Networks
Power-Performance Characterization of TinyML Systems
 Hyperdimensional Hybrid Learning on End-Edge-Cloud Networks

Session 11B: Networks and Large Systems

Equivalence Checking for Flow-Based Computing Sven Thijssen (University of Central Florida, USA), Sumit Kumar Jha (University of Texas at San Antonio, USA), and Rickard Ewetz (University of Central Florida, USA)	. 656
A Stripe-Schedule Aware Repair Technique in the Heterogeneous Network for Erasure-Coded Clusters	664
Hai Zhou (Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, China), Dan Feng (Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, China), and Yuchong Hu (School of Computer Science and Technology, Huazhong University of Science and Technology, China)	

Tear Up the Bubble Boom: Lessons Learned From a Deep Learning Research and Development Cluster	. 672
Zehua Yang (Peking University; Peng Cheng Laboratory), Zhisheng Ye	
(Peking University; Peng Cheng Laboratory), Tianhao Fu (Peking	
University), Jing Luo (Wuhan Textile University), Xiong Wei (Wuhan	
Textile University), Yingwei Luo (Peking University; Peng Cheng	
Laboratory), Xiaolin Wang (Peking University; Peng Cheng Laboratory),	
Zhenlin Wang (Michigan Tech University), and Tianwei Zhang (Nanyang	
Technological University)	
RCS: A Redirection Computational Scheduler to Accelerate Straggler Recovery for Erasure	
Coded Cloud Storage System	681
Xinzhe Cao (Shanghai Jiao Tong University, China), Yunfei Gu (Shanghai	
Jiao Tong University, China), Chentao Wu (Shanghai Jiao Tong	
University, China), Jie Li (Shanghai Jiao Tong University, China),	
Minyi Guo (Shanghai Jiao Tong University, China), Yuanyuan Dong (The	
Alibaba Group, China), and Yafei Zhao (The Alibabab Group, China)	

Session 12A: Memory Technologies

A Study of STT-RAM-Based In-Memory Computing Across the Memory Hierarchy Dhruv Gajaria (University of Arizona, USA), Kevin Antony Gomez (University of Arizona, USA), and Tosiron Adegbija (University of Arizona, USA)	685
Energy-Efficient Bus Encoding Techniques for Next-Generation PAM-4 DRAM Interfaces Youri Su (Hanyang University, Republic of Korea), Sanghun Lee (Hanyang University, Republic of Korea), Eunji Song (Hanyang University, Republic of Korea), Dongha Kim (Hanyang University, Republic of Korea), Jaeduk Han (Hanyang University, Republic of Korea), and Hokeun Kim (Hanyang University, Republic of Korea)	693

А	Hybrid Spin-CMOS Flash ADC Based on Spin Hall Effect and Spin Transfer Torque
	Hamdam Ghanatian (Aarhus University Aarhus, Denmark), Hooman Farkhani
	(Aarhus University Aarhus, Denmark), and Farshad Moradi (Aarhus
	University Aarhus, Denmark)

Session 12B: GPU and Memories

LAK: A Low-Overhead Lock-and-Key Based Schema for GPU Memory Safety	705
Chaochao Zhang (Institute of Information Engineering, Chinese Academy	
of Sciences; University of Chinese Academy of Sciences, China) and Rui	
Hou (Institute of Information Engineering, Chinese Academy of	
Sciences; University of Chinese Academy of Sciences, China)	

RMMIO: Enabling Reliable Memory-Mapped I/O for Persistent Memory Systems	722
Bo Ding (Huazhong University of Science and Technology, China), Wei	
Tong (Huazhong University of Science and Technology, China), Yu Hua	
(Huazhong University of Science and Technology, China), Zhangyu Chen	
(Huazhong University of Science and Technology, China), Xueliang Wei	
(Huazhong University of Science and Technology, China), and Dan Feng	
(Huazhong University of Science and Technology, China)	
CADedup: High-Performance Consistency-Aware Deduplication Based on Persistent Memory	726

 CADedup: High-Pertormance Consistency-Aware Deduplication Based on Persistent Memory 726 Chunlin Song (Chongqing University), Xianzhang Chen (Chongqing University), Duo Liu (Chongqing University), Xiaoliu Feng (Chongqing University), Xi Yu (Chongqing University), Jiali Li (Chongqing University), Yujuan Tan (Chongqing University), and Ao Ren (Chongqing University)

Session 13A: System Design

 GCNTrain: A Unified and Efficient Accelerator for Graph Convolutional Neural Network Training
Nesting Forward Automatic Differentiation for Memory-Efficient Deep Neural Network Training
Cong Guo (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute), Yuxian Qiu (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute), Jingwen Leng (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute), Chen Zhang (Alibaba Group, China), Ying Cao (Microsoft Research, China), Quanlu Zhang (Microsoft Research, China), Yunxin Liu (Institute for AI Industry Research, Tsinghua University, China), Fan Yang (Microsoft Research, China), and Minyi Guo (Shanghai Jiao Tong University; Shanghai Qi Zhi Institute)
 SOMALib : Library of Exact and Approximate Activation Functions for Hardware-Efficient Neural Network Accelerators

Session 13B: Emerging Computing Systems

Energy-Efficient Oriented Approximate Quantization Scheme for Fine-Grained Sparse Neural Network Acceleration	762
Tianyang Yu (Nanjing University of Aeronautics and Astronautics Nanjing, China), Bi Wu (Nanjing University of Aeronautics and Astronautics Nanjing, China), Ke Chen (Nanjing University of Aeronautics and Astronautics Nanjing, China), Chenggang Yan (Nanjing University of Aeronautics and Astronautics Nanjing, China), and Weiqiang Liu (Nanjing University of Aeronautics and Astronautics Nanjing, China)	
TizBin: A Low-Power Image Sensor with Event and Object Detection Using Efficient Processing-in-Pixel Schemes	770

Author Index	 	 	 	
Author Index	 • • • • • • • •	 	 	