

2022 IEEE 39th International Electronics Manufacturing Technology Conference (IEMT 2022)

**Kuala Lumpur, Putrajaya, Malaysia
19-21 October 2022**



**IEEE Catalog Number: CFP22IEU-POD
ISBN: 978-1-6654-7171-8**

**Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP22IEU-POD
ISBN (Print-On-Demand):	978-1-6654-7171-8
ISBN (Online):	978-1-6654-7170-1

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

Enable Detection and Classification of Abnormal Molding Process Through Systematic Advanced Process Control (APC) <i>Cheng Guan Ong, Siew Fen Ang, Wei Keong Ng</i>	1
Semiconductor Manufacturing Case Studies: Wedge Bonder Characterization via Advanced Process Control (APC) <i>Cheng Guan Ong, Sue Yin Seet, Nazaruddin Md Shah, Zamil Ezzuddin</i>	4
Modified Multipoint Constraints of Finite Element Model for SJR Prediction Accuracy <i>Ting-Wen Chen, Muhammad Zulfadhli Bin Bakhtiar, Shin-Yueh Yang, Yeow Chon Ong, Christopher Glancey, Hem Takiar</i>	6
Single Side Direct Cooling SiC Module Baseplate Warpage Behavior and Solutions..... <i>Raymund Nonato Concepcion, Jenelyn Rodriguez</i>	11
Solvent Cleaning to Clean Die from Fluorine After BOSCH Plasma Dicing <i>Mohd Akbar Md Sum, Jeongpyo Hong</i>	16
SSDC SiC Mosfet Panel Warpage Challenges at Sintering Process <i>Jenelyn Simbulan Rodriguez, Faiz Zuhairy Redzuan, Raymund Nonato Jotea Concepcion</i>	19
Critical Cleaning Requirements to Overcome Advanced Packaging Defluxing Challenges..... <i>Guan Tatt Yeoh, Ravi Parthasarathy</i>	25
Detailed Analysis of Conductive Die Attach Film in Miniature Package X3DFN <i>Meng Fatt Wan, Ying Heong Chiew, Yong Yuen Tey</i>	37
Package Fault Isolation for Low Density and Non-Metallic Particle Analysis <i>Saraswathy Supramaniam, Muhammad Nurhisham Bin Abdullah, Subashini Periasamyline</i>	42
Voltage Bias Enhancement for Leakage Test on Discrete Products to Detect Low Contact..... <i>Nik Ahmad Nizam Bin Nik Zainuddin, Nur Yashidar Binti Mohamad Yasin, Nur Syazreen Binti Ardnan, Chee Keat Gan, Mohd Fakrul Naim Bin Muhammad Zin, Azman Jalar</i>	48
Glass Dicing Process Optimization on Coated Borosilicate Glass for iBGA Product..... <i>May May Gan, Ying Heong Chiew</i>	53
Automation of AC Inductive Switching Characterization Data Acquisition using LabVIEW Software <i>Nurul Afiqah Mohd Hasbullah, Aik Wan Chan, Jingle Navarra</i>	60
Post Plate Bake as the Electronic Package Corrosion Firewall <i>Aiman Hakim Badarisman, Hamizan Ideris, Khirullah Abdul Hamid</i>	66
Effect of Wafer Back Metal Thickness and Surface Roughness Towards Backend Assembly Processes <i>Zi Ming Chang, Hui Min Ler</i>	70
Patent Landscape of Sintered Cu and Ag as Die-Attach Materials in Microelectronics Packaging <i>Kim S Siow</i>	80

Machine Learning Prediction Model for Automation Equipment Control in Semiconductor Manufacturing	84
<i>Amri Abu Bakar</i>	
The Investigation of Foldable Display Form Factor Notebook System & the Design Challenges.....	90
<i>Jia Yan Go, Chee How Lim, Jon Sern Lim, Yew San Lim, Khai Ern See, Vivek Paranjape</i>	
Wire Bond Qualification Challenges and Development of First Silver (Ag) Alloy Wire on Clip Bond Surface Mount Package	94
<i>Jeriel Figueroa, Swee Har Khor</i>	
Remote System in Semiconductor Industry	103
<i>Muhamad Nazir Bin Mislan</i>	
Correlation Study Between Pure Tin Plating Intermetallic and Grain Size.....	106
<i>Ronizan Mohd Salleh, Rasli Idris, Lim Koo Foong, Salazar Esperidion De Castro</i>	
Top Gate Molding Wire Sweep Improvement in QFP Exposes Pad Packages	111
<i>Chua Boo Wei</i>	
Backside Chipping Investigation & Improvement on TiNiVAg Back Metal Silicon Die.....	115
<i>Mohd Khairul Bin Zainal, Aswafi Bin Abdul Aziz, Vegneswary Ramalingam</i>	
Effects of Underfill Materials on Behavior of Intermetallic Compound Thickness of Ball Grid Array Solder Joints using ANOVA	119
<i>Adlil Aizat Ismail, Maria Abu Bakar, Abang Annuar Ehsan, Azman Jalar, Fakhrozi Che Ani, Zol Effendi Zolkefli</i>	
Intermetallic Compound Thickness of Ball Grid Array Solder Joints Under Thermal Cycling Test using ANOVA.....	124
<i>Adlil Aizat Ismail, Maria Abu Bakar, Abang Annuar Ehsan, Azman Jalar, Erwan Basiron, Fakhrozi Che Ani</i>	
A Novel High-Temperature Pb-Free Solder Paste with Enhanced Performance for Power Discrete Packaging Applications	128
<i>Hongwen Zhang, Sze Pei Lim, Samuel Lytwynec, Tyler Richmond, Tybarius Harter, Diego Prado</i>	
Sidewall Crack Improvement in the Mechanical Wafer Dicing Process.....	132
<i>Shazealina Abd Sukor</i>	
Low Peel Strength Investigation in Direct Gold System in Package Module	135
<i>Tsung Nan Lo, Wei Liu, Aldy Macatangay, Jaynal Molla, Pey Fang Hiew</i>	
Methodology of Development Robust 2nd Bond on Ultra-Thin Plating.....	139
<i>Nurhashimah Hashim, Kiangwei Quek, Muhammadhariz Mohamad Razip</i>	
WLCSP Descum Process Criticality and Its Impact on Leakage Performance	143
<i>Lau Teck Beng, Chofu Liu Yu Fu, Yujun Choi, Frank Swartjes, Myungjin Lim, Won Seok Oh, Martin Shin</i>	
Dual Row QFN Roughen Lead Frame Mold Flash Challenges & Resolution	148
<i>Pey Fang Hiew, Poh Leng Eu, Kirk Hsieh, Tinalt Chen, Milo Yang, Jaco Chan, Taitien Wang, Handsome Huang</i>	
Influence of Ball Grid Array Design Parameters on Solder Joint Reliability.....	152
<i>Amirul Afripin, Torsten Hauck</i>	

Strip Form Package Marking Challenges for Small Outline Packages	158
<i>Kow Siew Ting, Mohd Rozaini Mohd Zali, Muhd Firdaus Bin Mahat</i>	
Antimixing Flow for Small Outline Packages.....	162
<i>Kow Siew Ting, Wong Chan Leong, Geok Hau E</i>	
Investigation of Solder Void Improvement on Automotive Parts	166
<i>Aranas Guadalquever Brian, Pavendhran Chinathamby, Wing Onn Chaw, Ting Wei Chang</i>	
Cu Pillar Bump Oxidation Control in Flip Chip Package.....	169
<i>Wen Yuan Chuang, Wen Hung Huang, Eu Poh Leng, Taiyu Chen</i>	
Transfer Molding Wire Sweep Improvement in QFP Packages by Mold Plunger Tips Design.....	172
<i>Alvin Tan Kian Siang</i>	
Virtual Prototyping Approach for Package Delamination Risk Assessment Under Simulated High Temperature Exposure using Finite Element Analysis.....	176
<i>Rasydan Tahir, Zhang Bingbing</i>	
Application of Simulation to Enhance Complex Clipbond Package Mold Tools	182
<i>Vegneswary Ramalingam, Kow Siew Ting</i>	
Solder Extrusion Characterization Study on SiP Modules Inductors	186
<i>Antonio A. M. Macatangay, Jae Yun Kim, Poh Leng Eu, Sungwon Choi, Seongkuk Kang, Eunseong Go</i>	
Effect of Solder Voids on Chip Crack During Al Ribbon Bonding	189
<i>Chee Mun Wai, Comadre Ryan Tordillo, Bajuri Mohd Kahar, Jocson Emil Lamco, Selorio Edmund Banogon</i>	
Thermo-Mechanical Modeling to Analyze Package Stress of QFN Package.....	193
<i>KH Loh Rosazlan</i>	
MIS Strip Warpage Improvement by FEA Study.....	197
<i>SK Chin</i>	
Electrical Characterization of CZTS Thin Film Prepared by High Power Impulse Magnetron Sputtering (HiPIMS) Deposition	204
<i>Siti Noryasmin Jaffar, Nafarizal Nayan, Saidur Rahman, Mohd Khairul Ahmad</i>	
Ultra-Fine SAC305 Solder Paste Interconnection Solution for Advanced Packaging	209
<i>Lim Chze Min Jason, B. Senthil Kumar, Kang Sungsig, Yam Lip Huei, Zhang Rui Fen, Sarangapani Murali</i>	
Unit Level Traceability (ULT) Development and Implementation for High Level Traceability in Semicon Assembly & Test Manufacturing.....	214
<i>SP Oh, ST Choh, CD Ng, HK Phang</i>	
Advanced Assembly Technology for Small Chip Size of Fan-Out WLP using High Expansion Tape	218
<i>Tadatomo Yamada, Ken Takano, Toshiaki Menjo, Shinya Takyu</i>	
Co-Design of Intermittent Jet and Surface Structure for Heat Sink Cooling Enhancement	223
<i>Xincheng Wu, An Zou, Zhaoguang Wang, Qiang Zhang</i>	
Mining EDS-EBSD Data to Study Microstructure of Solder Bump with Completely Unknown Intermetallics	230
<i>Jiang Wu, Eugene Choo</i>	

On the JEDEC Board Level Drop Test Simulation of Array of BGA Packages	234
<i>Yiyi Ma, Jing-En Luan</i>	
Modeling & Investigating Packaging Effects on Sensing Devices.....	240
<i>Roseanne Duca</i>	
Hybrid GNPs/Silane Functionalised BN Composite as TIM: Thermal, Shear Strength and Moisture Analysis.....	245
<i>S. Jasmee, G. Omar, S. S. Che Othaman</i>	
A Novel High-Temperature Pb-Free Solder Paste with Enhanced Performance for Power Discrete Packaging Applications	256
<i>Hongwen Zhang, Sze Pei Lim, Samuel Lytwynec, Tyler Richmond, Tybarius Harter, Diego Prado</i>	

Author Index