

# **2022 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2022)**

**Shanghai, China  
7 – 14 October 2022**



**IEEE Catalog Number: CFP22COD-POD  
ISBN: 978-1-6654-7295-1**

**Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP22COD-POD
ISBN (Print-On-Demand):	978-1-6654-7295-1
ISBN (Online):	978-1-6654-7294-4
ISSN:	2832-6466

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# 2022 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) **CODES-ISSS 2022**

## Table of Contents

Welcome Message from the CODES+ISSS 2022 Program Chairs .....	vii
CODES+ISSS 2022 Program Committee .....	viii

### CODES+ISSS Work-in-Progress

Work-in-Progress: What to Expect of Early Training Statistics? An Investigation on Hardware-Aware Neural Architecture Search .....	1
<i>Xiangzhong Luo (Nanyang Technological University, Singapore), Di Liu (Nanyang Technological University, Singapore), Hao Kong (Nanyang Technological University, Singapore), Shuo Huai (Nanyang Technological University, Singapore), Hui Chen (Nanyang Technological University, Singapore), and Weichen Liu (Nanyang Technological University, Singapore)</i>	
Work-in-Progress: Scheduler for Collaborated FPGA-GPU-CPU Based on Intermediate Language ....	3
<i>Nan Hu (University of Science and Technology of China, China), Chao Wang (University of Science and Technology of China, China), Xuehai Zhou (University of Science and Technology of China, China), and Xi Li (University of Science and Technology of China, China)</i>	
Work-in-Progress: High-Performance Systolic Hardware Accelerator for RBLWE-Based Post-Quantum Cryptography .....	5
<i>Tianyou Bao (Villanova University, USA), José L. Imaña (Complutense University, Spain), Pengzhou He (Villanova University, USA), and Jiafeng Xie (Villanova University, USA)</i>	
Work-in-Progress: BloCirNN: An Efficient Software/hardware Codesign Approach for Neural Network Accelerators with Block-Circulant Matrix .....	7
<i>Yunji Qin (University of Science and Technology of China, China), Lei Gong (University of Science and Technology of China, China), Zhendong Zheng (University of Science and Technology of China, China), and Chao Wang (University of Science and Technology of China, China)</i>	
Work-in-Progress: HeteroRW: A Generalized and Efficient Framework for Random Walks in Graph Analysis .....	9
<i>Yingxue Gao (University Of Science And Technology of China, China), Lei Gong (University Of Science And Technology of China, China), Chao Wang (University Of Science And Technology of China, China), and Xuehai Zhou (University Of Science And Technology of China, China)</i>	

Work-in-Progress: Lark: A Learned Secondary Index Toward LSM-Tree for Resource-Constrained Embedded Storage Systems .....	11
<i>Jianan Yuan (Shenzhen University, China), Huan Liu (Shenzhen University, China), Shangyu Wu (City University of Hong Kong, China), Yiquan Lin (Shenzhen University, China), Tiantian Wang (Shenzhen University, China), Chenlin Ma (Shenzhen University, China), Rui Mao (Shenzhen University, China), and Yi Wang (Shenzhen University, China)</i>	
Work-in-Progress: Toward Energy-Efficient Near STT-MRAM Processing Architecture for Neural Networks .....	13
<i>Yueting Li (Beihang University, China), Bingluo Zhao (Beihang University, Beijing, China), Xinyi Xu (Beihang University, China), Yundong Zhang (Vimicro Corporation, Beijing, China), Jun Wang (Beihang University, China), and Weisheng Zhao (Beihang University, China)</i>	
Work-in-Progress: Utilizing Latency and Accuracy Predictors for Efficient Hardware-Aware NAS .....	15
<i>Negin Firouzian (McGill University, Canada), Seyyed Hasan Mozafari (McGill University, Canada), James J. Clark (McGill University, Canada), Warren J. Gross (McGill University, Canada), and Brett H. Meyer (McGill University, Canada)</i>	

## Industry Track

Industry-Track: Towards Agile Design of Neural Processing Unit .....	17
<i>Binyi Wu (Technische Universität Dresden, Germany), Wolfgang Furtner (Infineon Technologies AG, Germany), Bernd Waschneck (Infineon Technologies AG, Germany), and Christian Mayr (Technische Universität Dresden, Germany)</i>	
Industry Paper: Surrogate Models for Testing Analog Designs Under Limited Budget — A Bandgap Case Study .....	21
<i>Roderick Bloem (Graz University of Technology, Austria), Alberto Larrauri (Graz University of Technology, Austria), Roland Lengfeldner (Infineon Technologies AG, Austria), Cristinel Mateis (Austrian Institute of Technology, Austria), Dejan Nicković (Austrian Institute of Technology, Austria), and Björn Ziegler (Infineon Technologies AG, Austria)</i>	

## Special Session

Invited Paper: Brain-Inspired Hyperdimensional Computing for Ultra-Efficient Edge AI .....	25
<i>Hussam Amrouch (University of Stuttgart, Germany), Mohsen Imani (Bio-Inspired Architecture and Systems (BIASLab), UC Irvine, California, USA), Xun Jiao (Dependable, Efficient, and Intelligent Computing Lab (DETAIL), Villanova University, USA), Yiannis Aloimonos (Perception and Robotics Group, University of Maryland, USA), Cornelia Fermüller (Perception and Robotics Group, University of Maryland, USA), Dehao Yuan (Perception and Robotics Group, University of Maryland, USA), Dongning Ma (Dependable, Efficient, and Intelligent Computing Lab (DETAIL), Villanova University, USA), Hamza E. Barkam (Bio-Inspired Architecture and Systems (BIASLab), UC Irvine, California, USA), Paul R. Genssler (University of Stuttgart, Germany), and Peter Sutor (Perception and Robotics Group, University of Maryland, USA)</i>	

Author Index .....	35
--------------------	----