2022 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2022)

Shanghai, China
7-14 October 2022

IEEE Catalog Number: CFP22CCS-POD
ISBN: 978-1-6654-7297-5

Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP22CCS-POD
ISBN (Print-On-Demand):	978-1-6654-7297-5
ISBN (Online):	978-1-6654-7296-8
ISSN:	2381-1560

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

2022 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)

CASES 2022

Table of Contents

Welcome Message from the CASES 2022 Program Chairs ..... **ix**
CASES 2022 Program Committee ..... **x**

CASES Work-in-Progress

Work-in-Progress: Reliability Evaluation of Power SCADA System with Three-Layer IDS 1
Yenan Chen (Shanghai Jiao Tong University, China), Linsen Li (Shanghai Jiao Tong University, China), Zhaoqian Zhu (Shanghai Jiao Tong University, China), and Yue Wu (Shanghai Jiao Tong University, China)

Work-in-Progress: MLGOPerf: An ML Guided Inliner to Optimize Performance 3
Amir H. Ashouri (Huawei Technologies, Canada), Mostafa Elhoushi (Huawei Technologies, Canada), Yuzhe Hua (Huawei Technologies, Canada), Xiang Wang (Huawei Technologies, Canada), Muhammad Asif Manzoor (Huawei Technologies, Canada), Bryan Chan (Huawei Technologies, Canada), and Yaoqing Gao (Huawei Technologies, Canada)

Work in Progress: ACAC: An Adaptive Congestion-Aware Approximate Communication Mechanism for Network-on-Chip Systems 5
Shize Zhou (Nanjing University, China), Yongqi Xue (Nanjing University, China), Siyue Li (Nanjing University, China), Jinlun Ji (Nanjing University, China), Tong Cheng (Nanjing University, China), Li Li (Nanjing University, China), and Yuxiang Fu (Nanjing University, China)

Work-in-Progress: ExpCache: Online-Learning Based Cache Replacement Policy for Non-Volatile Memory 7
Jinfeng Yang (University of Minnesota), Bingzhe Li (Oklahoma State University), Jianjun Yuan (Expedia Group), Zhaoyan Shen (Shandong University), David Du (University of Minnesota), and David Lilja (University of Minnesota)

Work-in-Progress: On Evaluation of On-Chip Thermal Covert Channel Attacks 9
Jiachen Wang (South China University of Technology, China), Xiaohang Wang (South China University of Technology, China), Yingtao Jiang (Unversity of Nevada Las Vegas), Amit Kumar Singh (University of Essex, UK), Letian Huang (University of Electronic Science and Technology of China, China), and Mei Yang (Unversity of Nevada Las Vegas)

Work-in-Progress: High-Precision Short-Term Lifetime Prediction in TLC 3D NAND Flash Memory as Hot-Data Storage 11
Xiaotong Fang (Shandong University, China), Meng Zhang (Huazhong University of Science and Technology, China), Yifan Guo (Shandong University, China), Fei Chen (Shandong University, China), Binglu Chen (Shandong University, China), Xuepeng Zhan (Shandong University, China), Jixuan Wu (Shandong University, China), Fei Wu (Huazhong University of Science and Technology, China), and Jiezhi Chen (Shandong University, China)

Work-in-Progress: Prediction-Based Fine-Grained LDPC Reading to Enhance High-Density Flash Read Performance 13
Yajuan Du (Wuhan University of Technology, China), Yuan Gao (Wuhan University of Technology, China), and Qiao Li (Xiamen University, China)

Work-in-Progress: Object Detection Acceleration Method by Improving Execution Efficiency of AI Device 15
Yoshikazu Watanabe (NEC Corporation, Japan), Yuki Kobayashi (NEC Corporation, Japan), Noboru Nakajima (NEC Solution Innovators, Japan), Takashi Takenaka (NEC Corporation, Japan), and Hiroyoshi Miyano (NEC Corporation, Japan)

Work-in-Progress: Toward a Robust, Reconfigurable Hardware Accelerator for Tree-Based Genetic Programming 17
Christopher Crary (University of Florida, USA), Wesley Piard (University of Florida, USA), Britton Chesley (University of Florida, USA), and Greg Stitt (University of Florida, USA)

Work-in-Progress: Towards a Smaller than Grain Stream Cipher: Optimized FPGA Implementations of Fruit-80 19
Gangqiang Yang (Shandong University, China), Zhengyuan Shi (Shandong University, China), Cheng Chen (Shandong University, China), Hailiang Xiong (Shandong University, China), Honggang Hu (University of Science and Technology of China, China), Zhiguo Wan (Zhejiang Lab, China), Keke Gai (Beijing Institute of Technology, China), and Meikang Qiu (Texas A&M University-Commerce, USA)

Work-in-Progress: CAMiSE: Content Addressable Memory-Integrated Searchable Encryption 21
Arnab Bag (Indian Institute of Technology Kharagpur, India), Sikhar Patranabis (ETH Zurich, Switzerland), and Debdeep Mukhopadhyay (Indian Institute of Technology Kharagpur, India)

Work-in-Progress: Smart Data Reduction in SLAM Methods for Embedded Systems 23
Quentin Picard (CEA, LIST, France), Stephane Chevobbe (CEA, LIST, France), Mehdi Darouich (CEA, LIST, France), Zoe Mandelli (CEA, LIST, France), Mathieu Carrier (CEA, LIST, France), and Jean-Yves Didier (IBISC, Univ Evry, Université Paris-Saclay, France)

Work-in-Progress: An Open-Source Platform for Design and Programming of Partially Reconfigurable Heterogeneous SoCs 25
Biruk Seyoum (Columbia University, USA), Davide Giri (Columbia University, USA), Kuan-Lin Chiu (Columbia University, USA), and Luca Carloni (Columbia University, USA)

Work-in-Progress: Ultra-Fast yet Accurate Performance Prediction for Deep Neural Network Accelerators 27
Konstantin Lübeck (University of Tübingen, Germany), Alexander Louis-Ferdinand Jung (University of Tübingen, Germany), Felix Wedlich (University of Tübingen, Germany), and Oliver Bringmann (University of Tübingen, Germany)

Work-in-Progress: Cooperative MLP-Mixer Networks Inference On Heterogeneous Edge Devices Through Partition and Fusion 29
Yiming Li (East China Normal University, China), Shouzhen Gu (East China Normal University, China), and Mingsong Chen (East China Normal University, China)

Work-in-Progress: RISC-V Based Low-Cost Embedded Trace Processing System 31
Xiao Hu (National University of Defense Technology, China), Yaohua Wang (National University of Defense Technology, China), and Xuan Gao (National University of Defense Technology, China)

Work-in-Progress: Efficient Low-Latency Near-Memory Addition 33
Alexander Reaugh (University of Kentucky, USA) and Sayed Ahmad Salehi (University of Kentucky, USA)

Work-in-Progress: SuperNAS: Fast Multi-objective SuperNet Architecture Search for Semantic Segmentation 35
Marihan Amein (McGill University, Canada), Zhuoran Xiong (McGill University, Canada), Olivier Therrien (McGill University, Canada), Brett H. Meyer (McGill University, Canada), and Warren J. Gross (McGill University, Canada)

Work-in-Progress: A Processing-in-Pixel Accelerator Based on Multi-level HfOx ReRAM 37
Minhaz Abedin (SUNY Polytechnic Institute, USA), Arman Roohi (University of Nebraska–Lincoln, USA), Nathaniel Cady (SUNY Polytechnic Institute, USA), and Shaahin Angizi (New Jersey Institute of Technology, USA)

Work in Progress: Emulation of Biological Tissues on an FPGA 39
Jerry Jacob (University of Auckland, New Zealand), Sucheta Sehgal (University of Auckland, New Zealand), and Nitish Patel (University of Auckland, New Zealand)

Work-in-Progress: DRAM-MaUT: DRAM Address Mapping Unveiling Tool for ARM Devices 41
Anandpreet Kaur (IIIT Allahabad, India), Pravin Srivastav (IIIT Allahabad, India), and Bibhas Ghoshal (IIIT Allahabad, India)

Work-in-Progress: NoRF: A Case Against Register File Operands in Tightly-Coupled Accelerators 43
David J. Schlais (University of Wisconsin-Madison), Heng Zhuo (University of Wisconsin-Madison), and Mikko H. Lipasti (University of Wisconsin-Madison)

Author Index **47**