2022 IEEE 72nd Electronic **Components and Technology** Conference (ECTC 2022)

San Diego, California, USA 31 May – 3 June 2022

Pages 1-779



IEEE Catalog Number: CFP22ECT-POD ISBN:

978-1-6654-7944-8

Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number: CFP22ECT-POD ISBN (Print-On-Demand): 978-1-6654-7944-8 ISBN (Online): 978-1-6654-7943-1

ISSN: 0569-5503

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA

Phone: (845) 758-0400 Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



2022 IEEE 72nd Electronic Components and Technology Conference (ECTC) ECTC 2022

Table of Contents

Foreword ECTC 2022 Executive Committee ECTC 2022 Program Committee	lxxii
Session 1: Advanced Packaging for Heterogeneous Integration High Performance Computing	and
Organic Interposer CoWoS-R + (plus) Technology M.L. Lin (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), M.S. Liu (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), H.W. Chen (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), S.M. Chen (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), M.C. Yew (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), C.S. Chen (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.)), and Shin-Puu Jeng (Taiwan Semiconductor Manufacturing Company, Taiwan (R.O.C.))	1
Cost-Effective RF Interposer Platform on low-Resistivity Si Enabling Heterogeneous Integration Opportunities for Beyond 5G Xiao Sun (Imec, Belgium), John Slabbekoorn (Imec, Belgium), Siddhartha Sinha (Imec, Belgium), Pieter Bex (Imec, Belgium), Nelson Pinho (Imec, Belgium), Tomas Webers (Imec, Belgium), Dimitrios Velenis (Imec, Belgium), Andy Miller (Imec, Belgium), Nadine Collaert (Imec, Belgium), Geert Van der Plas (Imec, Belgium), and Eric Beyne (Imec, Belgium)	7
Chiplet-based System PSI Optimization for 2.5D/3D Advanced Packaging Implementation Yoonjae Hwang (Samsung Electronics, South Korea), Sungwook Moon (Samsung Electronics, South Korea), Seungki Nam (Samsung Electronics, South Korea), and Jeong Hoon Ahn (Samsung Electronics, South Korea)	.12
Double Side SiP of Structure Strength Analysis for 5G and Wearable Application	. 18

A Laser Dicing Method for Plus-Shaped Dies for Heterogenous Integration Applications	4
2.3D Hybrid Substrate with Ajinomoto Build-Up Film for Heterogeneous Integration	0
Advanced Packaging Technologies for Co-Packaged Optics	8
Session 2: High Performance Dielectric Materials for Advanced Packaging	
Ultra-thin mold cap for Advanced Packaging Technology	.3
Evaluation of the Transmission Loss of Soluble Polyphenylene Ether Composite Material in a Millimeter-Wave Region	51

Low-Dielectric, Low-Profile IC Substrate Material Development for 5G Applications	56
Reliability Assessment of Ultra-low-K Dielectric Material and Demonstration in Advanced Interposers Pragna Bhaskar (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Christopher Blancher (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Mohan Kathaperumal (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Madhavan Swaminathan (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), and Mark D. Losego (3D Systems Packaging Research Center, Georgia Institute of Technology, USA)	62
Low Dielectric New Resin Cross-Linkers	67
Solid-Diffusion Synthesis of Robust Hollow Silica Filler with low Dk and low Df	71
Epoxy Wetting Flow and Adhesion Mechanism Within a Small Gap and Small Pitch Copper Pil Structure Mary-Ann Gasser (Université Grenoble Alpes, CEA Leti, France), Abdenacer Ait Mani (Université Grenoble Alpes, CEA Leti, France), Thierry Mourier (Université Grenoble Alpes, CEA Leti, France), Alain Gueugnot (Université Grenoble Alpes, CEA Leti, France), Patrick Peray (Université Grenoble Alpes, CEA Leti, France), Loïc Vanel (Université de Lyon, Université Claude Bernard Lyon 1, CNRS-Institut Lumière Matière, France), and Catherine Barentin (Université de Lyon, Université Claude Bernard Lyon 1, CNRS-Institut Lumière Matière, France)	

Session 3: Antenna-in-Package for Communication, Radar and Energy Transfer

77GHz Cavity-Backed AiP Array in FOWLP Technology Mei Sun (Institute of Microelectronics (IME), ASTAR(Agency for Science, Technology and Research), Singapore), Lim Teck Guan (Institute of Microelectronics (IME), ASTAR(Agency for Science, Technology and Research), Singapore), and Chai Tai Chong (Institute of Microelectronics (IME), ASTAR(Agency for Science, Technology and Research), Singapore)	82
Smart" Packaging of Self-Identifying and Localizable mmID for Digital Twinning and	
Metaverse Temperature Sensing Applications	. 87
A Planar High-Efficient W-Band Substrate-Integrated-Waveguide Cavity-Backed Slot Antenna	
Array	. 93
Compact Frequency Reconfigurable Array Antenna Based on Diagonally Placed Meander-Line Decouplers and PIN Diodes for Multi-range Wireless Communications	
High Gain and Low Back Radiation and Thin Antenna Designs using Electromagnetic Bandgap Surface for Radar and Wearable Applications	
Reconfigurable Antennas and FSS with Magnetically-Tunable Multiferroic Components Pawan Gaire (Florida International University, USA), John L. Volakis (Florida International University, USA), Shubhendu Bhardwaj (Florida International University, USA), Veeru Jaiswal (Florida International University, USA), and Markondeya Raj Pulugurtha (Florida International University, USA)	109
Electrically Small Folded Spherical Helix Antennas Utilizing Thick Solution Cast Nanomagnetic Films Nicholas Sturim (Michigan State University, USA), Edgar Aldama (Georgia Institute of Technology, USA), Eric Drew (Georgia Institute of Technology, USA), John Z. Zhang (Georgia Institute of Technology, USA), and John Papapolymerou (Michigan State University, USA)	116

Session 4: Hybrid Bonding and Innovations for 3D Integration

3-Layer Stacking Technology with Pixel-Wise Interconnections for Image Sensors using Hybrid Bonding of Silicon-on-Insulator Wafers Mediated by Thin Si Layers	122
Wafer to Wafer Hybrid Bonding for DRAM Applications Jinwon Park (SK Hynix Semiconductor Co., LTD, Republic of Korea), Byungho Lee (SK Hynix Semiconductor Co., LTD, Republic of Korea), Heesun Lee (SK Hynix Semiconductor Co., LTD, Republic of Korea), Dail Rim (SK Hynix Semiconductor Co., LTD, Republic of Korea), Jiho Kang (SK Hynix Semiconductor Co., LTD, Republic of Korea), Changhyun Cho (SK Hynix Semiconductor Co., LTD, Republic of Korea), Myunghee Na (SK Hynix Semiconductor Co., LTD, Republic of Korea), and Ilsup Jin (SK Hynix Semiconductor Co., LTD, Republic of Korea)	126
Analysis of Die Edge Bond Pads in Hybrid Bonded Multi-die Stacks Jeremy A. Theil (Xperi Corporation, USA), Thomas Workman (Xperi Corporation, USA), Dominik Suwito (Xperi Corporation, USA), Laura Mirkarimi (Xperi Corporation, USA), Gill Fountain (Xperi Corporation, USA), Km Bang (Xperi Corporation, USA), Guilian Gao (Xperi Corporation, USA), Bongsub Lee (Xperi Corporation, USA), Pawel Mrozek (Xperi Corporation, USA), Cyprian Uzoh (Xperi Corporation, USA), Michael Huynh (Xperi Corporation, USA), and Oliver Zhao (Xperi Corporation, USA)	130
The Integration of Grounding Plane into TSV Integrated Ion Trap for Efficient Thermal Management in Large Scale Quantum Computing Device	137
Wafer Stacked Wide I/O DRAM with One-Step TSV Technology Kawano Masaya (Institute of Microelectronics, Singapore), Xiangyu Wang (Institute of Microelectronics, Singapore), Qin Ren (Institute of Microelectronics, Singapore), Woon-Leng Loh (Institute of Microelectronics, Singapore), B.S.S. Chandra Rao (Institute of Microelectronics, Singapore), King-Jien Chui (Institute of Microelectronics, Singapore), Tsuyoshi Kawagoe (UltraMemory Inc., Japan), and Johiro Homma (UltraMemory Inc., Japan)	143

Recess Effect Study and Process Optimization of Sub-10 µm Pitch Die-to-wafer Hybrid Bonding
Haoxiang Ren (University of California, Los Angeles (UCLA), USA), Yu-Tao Yang (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), and Subramanian S. Iyer (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA)
A Performance Testing Method of Bernoulli Picker for Ultra-Thin Die Handling Application 157 Juno Kim (Samsung Electronics Co. Ltd., South Korea), Dae Ho Min (Samsung Electronics Co. Ltd., South Korea), Kangsan Lee (Samsung Electronics Co. Ltd., South Korea), Mingu Lee (Samsung Electronics Co. Ltd., South Korea), Kyeongbin Lim (Samsung Electronics Co. Ltd., South Korea), and Daniel Minwoo Rhee (Samsung Electronics Co. Ltd., South Korea)
Session 5: Bonding Technology: Novel Assembly Methods and Processes
The Influence of Cu Microstructure on Thermal Budget in Hybrid Bonding
Collective Die-to-Wafer Self-Assembly for High Alignment Accuracy and High Throughput 3D Integration
Fine-Pitch 30 µm Cu-Cu Bonding by using Low Temperature Microfluidic Electroless Interconnection
Die Bonding Solution for Flip Chip-Chip Scale Package- DIC (Digital Image Correlation) and Shadow Moiré Application

Bonding	187
Demin Liu (National Yang Ming Chiao Tung University, Taiwan), Kuan-Chun Mei (National Yang Ming Chiao Tung University, Taiwan), Han-Wen Hu (National Yang Ming Chiao Tung University, Taiwan), Yi-Chieh Tsai Tsai (National Yang Ming Chiao Tung University, Taiwan), Huang-Chung Cheng (National Yang Ming Chiao Tung University, Taiwan), and Kuan-Neng Chen Chen (National Yang Ming Chiao Tung University, Taiwan)	0,
Process and Design Optimization for Hybrid Cu Bonding Void	194
Laser-Assisted Bonding (LAB) Process and Its Bonding Materials as Technologies enabling the Low-Carbon Era	198
Session 6: Emerging Modeling Including AI and Machine Learnin	ıg
Applied Modeling Framework in Integrated Circuit Design and Reliability	204
Co-design of Thermal Management with System Architecture and Power Management for 3D IO 211 Rishav Roy (Purdue University, USA), Shidhartha Das (Arm Ltd., UK), Benoît Labbe (Arm Ltd., UK), Rahul Mathur (Arm Inc., USA), and Supreet Jeloka (Arm Inc., USA)	Cs.
On-Chip Transient Hot Spot Detection with a Multiscale ROM in 3DIC Designs	221

Implementation of Fully Coupled Electromigration Theory in COMSOL	.233
Peridynamic Modeling of non-Fourier and non-Fickian Diffusion in a Finite Element Framework S.V.K. Anicode (The University of Arizona, USA) and E Madenci (The University of Arizona, USA)	.239
Feature Vector Based Remaining Useful-Life Assessment in Mechanical Shock and Vibration for Leadfree Electronics	. 248
Genetic Algorithm–Assisted Design of Redistribution Layer Vias for a Fan-Out Panel-Level SiC MOSFET Power Module Packaging	. 260
Session 7: Advanced Flip Chip and Embedded Substrate Technologies	
Flip-Chip Chip Scale Package (FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7nm Si Technology	. 266
In-Package Ring Hybrid Coupler with On-chip Termination Trieb Robert (Division Engineering of Adaptive Systems, Germany) and Heinig Andy (Division Engineering of Adaptive Systems, Germany)	. 271

Superconducting Molybdenum Multi-chip Module Approach for Cryogenic and Quantum Applications Archit Shah (Auburn University, USA), Sherman E. Peek (Auburn University, USA), Bhargav Yelamanchili (Auburn University, USA), Vaibhav Gupta (Auburn University, USA), David B. Tuckerman (Tuckerman and Associates, Inc., USA), Chris Cantaloube (Microsoft Corporation, USA), John A. Sellers (Auburn University, USA), and Michael C. Hamilton (Auburn University, USA)	276
Functional Interposer Embedded with Multi-terminal Si Capacitor for 2.5D/3D Applications using Planarization and Bumpless Chip-on-Wafer (COW)	283
3D Embedded Power Package Module to Integrate Various Power Systems Byong Jin Kim (R&D, Amkor Technology Korea, Inc., Republic of Korea), Hyeongll Jeon (R&D, Amkor Technology Korea, Inc., Republic of Korea), DaeYoung Park (R&D, Amkor Technology Korea, Inc., Republic of Korea), Gi Jeong Kim (R&D, Amkor Technology Korea, Inc., Republic of Korea), Nam-Hee Cho (Materials Science and Engineering of Inha University, Republic of Korea), and Jin Young Khim (R&D, Amkor Technology Korea, Inc., Republic of Korea)	289
Demonstration of Substrate Embedded Ni-Zn Ferrite Core Solenoid Inductors using a Photosensitive Glass Substrate	. 296
Fabrication and Characterization of Package Embedded Inductors for Integrated Voltage Regulators Prahalad Murali (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Venkatesh Avula (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Marisa Ahmed (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Mark D. Losego (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Madhavan Swaminathan (3D Systems Packaging Research Center, Georgia Institute of Technology, USA), Claudio Alvarez (Intel Corporation, Chandler, USA), Yusuke Oishi (Panasonic Corporation), Tomohito Uemura (Panasonic Corporation), Ryo Nagatsuka (Panasonic Corporation), and Naoki Watanabe (Panasonic Industrial Device Sales Company of America)	301

Session 8: Hybrid and Direct Bonding Development and Characterization

Development of Face-to-Face and Face-to-Back Ultra-Fine Pitch Cu-Cu Hybrid Bonding	306
Surface Energy Characterization for Die-Level Cu Hybrid Bonding Katsuyuki Sakuma (IBM T.J. Watson Research Center, USA), Roy Yu (IBM T.J. Watson Research Center, USA), Michael Belyansky (IBM T.J. Watson Research Center, USA), Marc A. Bergendahl (IBM T.J. Watson Research Center, USA), Juan-Manuel Gomez (IBM T.J. Watson Research Center, USA), Spyridon Skordas (IBM T.J. Watson Research Center, USA), John Knickerbocker (IBM T.J. Watson Research Center, USA), Dale McHerron (IBM T.J. Watson Research Center, USA), Ming Li (ASM Pacific Technology, Hong Kong), Yiu Ming Cheung (ASM Pacific Technology, Hong Kong), Siu Cheung So (ASM Pacific Technology, Hong Kong), So Ying Kwok (ASM Pacific Technology, Hong Kong), Chun Ho Fan (ASM Pacific Technology, Hong Kong), and Siu Wing Lau (ASM Pacific Technology, Hong Kong)	312
Comprehensive Study on Advanced Chip on Wafer Hybrid Bonding with Copper/Polyimide Systems	317
Toshiaki Shirasaka (Showa Denko Materials Co., Ltd., Japan), Tadashi Okuda (Showa Denko Materials Co., Ltd., Japan), Tomoaki Shibata (Showa Denko Materials Co., Ltd., Japan), Satoshi Yoneda (HD MicroSystems, Ltd., Japan), Daisaku Matsukawa (HD MicroSystems, Ltd., Japan), Murugesan Mariappan (Tohoku University, Japan), Mitsumasa Koyanagi (Tohoku University, Japan), and Takafumi Fukushima (Tohoku University, Japan)	
Two-Step Ar/N_2 Plasma-Activated Al Surface for Al-Al Direct Bonding Liangxing Hu (Nanyang Technological University, Singapore), Yu Dian Lim (Nanyang Technological University, Singapore), Peng Zhao (Nanyang Technological University, Singapore), Michael Joo Zhong Lim (Nanyang Technological University, Singapore), and Chuan Seng Tan (Nanyang Technological University, Singapore; Jointly appointed at the Institute of Microelectronics, A*STAR, Singapore)	. 324
Novel Ga Assisted Low-Temperature Bonding Technology for Fine-Pitch Interconnects	. 330

Characterization of Die-to-Wafer Hybrid Bonding Using Heterogeneous Dielectrics
Solder and Organic Adhesive Hybrid Bonding Technology with Non-Strip Type Photosensitive Resin and Injection Molded Solder (IMS)
Chemicals, Inc., Japan), and Kazuo Kohmura (Mitsui Chemicals, Inc., Japan) Session 9: Millimeter-Wave Antenna-in-Package: Design,
Japan)
Session 9: Millimeter-Wave Antenna-in-Package: Design,
Session 9: Millimeter-Wave Antenna-in-Package: Design, Manufacturing and Test A 16 Element Antenna Integrated Package for 37-40GHz Operation

Multi-layer FCCSP Organic Packaging for D-band Millimeter Wave Applications	. 365
Slot Bow-Tie Antenna Integration in Flip-Chip and Embedded Die Enhanced QFN Package for WR8 and WR5 Frequency Band	
Antenna-Integrated, Die-Embedded Glass Package for 6G Wireless Applications	377
Design and Testing of a WR28 Waveguide Blind Mating Interconnect for mmWave ATE OTA Applications	384
Session 10: Novel Photonics Packaging Technology	
Demonstration of Fan-out Silicon Photonics Module for Next Generation Co-Packaged Optic (CPO) Application	s 394

3
0
2
8

Coupling Between Laser / Photodetector and Fiber Daiki Suemori (Keio University, Japan), Maho Ishii (Graduate School of Science and Technology, Keio University, Japan), Naohiro Kohmu (Graduate School of Science and Technology, Keio University, Japan), and Takaaki Ishigure (Keio University, Japan)	436
Lossless High-Speed Silicon Photonic MZI Switch with a Micro-Transfer-Printed III-V Amplifier Jing Zhang (Ghent University-imec, Belgium), Clemens J. Krückel (Ghent University-imec, Belgium), Bahawal Haq (Ghent University-imec, Belgium), Bozena Matuskova (EV Group E.Thallner GmbH, Austria), Johanna Rimbock (EV Group E.Thallner GmbH, Austria), Stefan Ertl (EV Group E.Thallner GmbH, Austria), Agnieszka Gocalinska (Tyndall National Institute University College Cork, Ireland), Emanuele Pelucchi (Tyndall National Institute University College Cork, Ireland), Brian Corbett (Tyndall National Institute University College Cork, Ireland), Joris Van Campenhout (IMEC, Belgium), Guy Lepage (IMEC, Belgium), Peter Verheyen (IMEC, Belgium), Dries Van Thourhout (Photonics Research Group, INTEC, Ghent University - imec, Belgium), and Gunther Roelkens (Photonics Research Group, INTEC, Ghent University - imec, Belgium)	441
Session 11: Automotive and Harsh Environment	
Cu-Al IMC Degradation under High Electric Fields during HTOL Tests A. Mavinkurve (NXP Semiconductors, The Netherlands), R.T.H. Rongen (NXP Semiconductors, The Netherlands), and M. van Soestbergen (NXP Semiconductors, The Netherlands)	446
Cu-Al IMC Degradation under High Electric Fields during HTOL Tests A. Mavinkurve (NXP Semiconductors, The Netherlands), R.T.H. Rongen (NXP Semiconductors, The Netherlands), and M. van Soestbergen (NXP Semiconductors, The Netherlands) Effect of Underfill Property Evolution on Solder Joint Reliability in Automotive	
Cu-Al IMC Degradation under High Electric Fields during HTOL Tests A. Mavinkurve (NXP Semiconductors, The Netherlands), R.T.H. Rongen (NXP Semiconductors, The Netherlands), and M. van Soestbergen (NXP Semiconductors, The Netherlands)	
Cu-Al IMC Degradation under High Electric Fields during HTOL Tests A. Mavinkurve (NXP Semiconductors, The Netherlands), R.T.H. Rongen (NXP Semiconductors, The Netherlands), and M. van Soestbergen (NXP Semiconductors, The Netherlands) Effect of Underfill Property Evolution on Solder Joint Reliability in Automotive Applications Pradeep Lall (Auburn University, USA), Madhu Kasturi (Auburn University, USA), Yunli Zhang (Auburn University, USA), Haotian Wu (Auburn University, USA), Jeff Suhling (Auburn University, USA), and	455

Fen Chen (Cruise LLC, USA), Gilberto Madrid (Cruise LLC, USA), Brian Schlotterbeck (Cruise LLC, USA), Jagdeep Singh (Cruise LLC, USA), Adli Nureddin (Cruise LLC, USA), Tyler Sawyer (Cruise LLC, USA), Zoran Stefanoski (Cruise LLC, USA), Spencer Klimpke (Cruise LLC, USA), Hector Guajardo (Cruise LLC, USA), Arul Ramalingam (Cruise LLC, USA), Maik Duwensee (Cruise LLC, USA), and Min Wang (Cruise LLC, USA)
Comprehensive Study of Long-Term Reliability of Copper Bonding Wires at Harsh Automotive Conditions
Post Wirebonding Coating for Prevention of Corrosion of Wire Bonded Packages by Chlorine Containing Foreign Particles
(NXP Semiconductors)
Session 12: Manufacturing and Assembly Process Modeling

Transient Thermal Modeling of Die Bond Process in Multiple Die Stacked Flash Memory Package	513
Yangming Liu (Western Digital Corporation, Package Technology Development and Integration, China), Xu Wang (Western Digital Corporation, Package Technology Development and Integration, China), Xiangyang Liu (Western Digital Corporation, Package Technology Development and Integration, China), Shenghua Huang (Western Digital Corporation, Package Technology Development and Integration, China), Chin-Tien Chiu (Western Digital Corporation, Package Technology Development and Integration, China), Ning Ye (Western Digital Corporation, Package Technology Development and Integration, USA), and Bo Yang (Western Digital Corporation, Package Technology Development and Integration, USA)	
Novel Method for NCF Flow Simulation in HBM Thermal Compression Bonding Process to Optimize the NCF Shape	519
Numerical Evaluation on SiO2 Based Chip to Wafer Hybrid Bonding Performance by Finite Element Analysis	524
A Novel Equivalent Model for Underfill Molding Process on 2.2 D Structure for High Performance Applications	. 531
Key Steps from Laboratory Towards mass Production: Optimization of Electroless Plating Process through Numerical Simulation	. 539

Session 13: Technologies for Heterogeneous Integration, Automotive and Power Electronics

Inductance	548
Chun-Kit Cheung (Hong Kong Applied Science and Technology Research Institute, China) and Ziyang Gao (Hong Kong Applied Science and Technology Research Institute, China)	
Static/Transient Thermal Analysis and Design Optimization of a Lead Frame Based Dual Side Cooling SiC Power Module	. 554
Kazunori Yamamoto (Institute of Microelectronics, A*STAR, Singapore) Impact of Reliability Tests on the Adhesion of the Epoxy Mold Compound David Guillon (Hitachi Energy, Switzerland), Andris Avots (Hitachi Energy, Switzerland), Milad Maleki (Hitachi Energy, Switzerland), Katrin Schlegel (Hitachi Energy, Switzerland), and Isabell Ehrler (Hitachi Energy, Switzerland)	. 561
Advanced Thermal Integration for HPC Packages with Two-Phase Immersion Cooling Po-Yao Lin (Taiwan Semiconductor Manufacturing Company, Taiwan), Sheng-Liang Kuo (Taiwan Semiconductor Manufacturing Company, Taiwan), Kathy Yan (Taiwan Semiconductor Manufacturing Company, Taiwan), Wen-Ming Chen (Taiwan Semiconductor Manufacturing Company, Taiwan), and Marvin De-Dui Liao (Taiwan Semiconductor Manufacturing Company, Taiwan)	. 566
Hybrid Stacked-Die Package Solution for Extremely Small-Form-Factor Package	574
Thermo-Mechanical Analysis of Thermal Compression Bonding Chip-Join Process	579
Dimensional Parameters Controlling Capillary Underfill Flow for Void-Free Encapsulation of a Direct Bonded Heterogeneous Integration (DBHi) Si-Bridge Pakcage	. 586

Session 14: Novel Bonding and and Stacking Technologies

Behavior of Bonding Strength on Wafer-to-Wafer Cu-Cu Hybrid Bonding Shunsuke Furuse (Sony Semiconductor Solutions Corporation, Japan), Nobutoshi Fujii (Sony Semiconductor Solutions Corporation, Japan), Kengo Kotoo (Sony Semiconductor Solutions Corporation, Japan), Naoki Ogawa (Sony Semiconductor Solutions Corporation, Japan), Suguru Saito (Sony Semiconductor Solutions Corporation, Japan), Taichi Yamada (Sony Semiconductor Solutions Corporation, Japan), Takaaki Hirano (Sony Semiconductor Solution Corporation, Japan), Yoshiya Hagimoto (Sony Semiconductor Solutions Corporation, Japan), and Hayato Iwamoto (Sony Semiconductor Solutions Corporation, Japan)	.591
Development of Polyimide Base Photosensitive Permanent Bonding Adhesive for Middle to L Temperature Hybrid Bonding Processes Satoshi Yoneda (HD MicroSystems, Ltd., Japan), Kenya Adachi (HD MicroSystems, Ltd., Japan), Daisaku Matsukawa (HD MicroSystems, Ltd., Japan), Takahiro Tanabe (HD MicroSystems, Ltd., Japan), Kaori Kobayashi (Showa Denko Materials Co., Ltd., Japan), Toshiaki Shirasaka (Showa Denko Materials Co., Ltd., Japan), Shizu Fukuzumi (Showa Denko Materials Co., Ltd., Japan), and Tadashi Okuda (Showa Denko Materials Co., Ltd., Japan)	.ow .595
Direct Bonding using Low Temperature SiCN Dielectrics	.602
Heterogeneous Integration by the 3D Stacking of Thin Silicon Die	. 608
Prolongation of the Surface Activation Effect using Self-Assembled Monolayer for Low Temperature Bonding of Au Kai Takeuchi (Collaborative Research Center, Meisei University, University of Tokyo, Japan), Beomjoon Kim (Institute of Industrial Science, University of Tokyo, Japan), and Tadatomo Suga (Meisei University, Japan)	. 614
Mini LED array transferred onto a flexible substrate using Simultaneous Transfer and Bonding (SITRAB) process and Anisotropic Solder Film (ASF)	. 619

Characterization of Non-Conductive Paste Materials (NCP) for Thermocompression Bonding a Direct Bonded Heterogeneously Integrated (DBHi) Si-Bridge Package	
Session 15: Enhanced Methods & Processes for Heterogeneous Integration Assembly	5
Super Fine Jet Underfill Dispense Technique for Robust Micro Joint in Direct Bonded Heterogeneous Integration (DBHi) Silicon Bridge Packages	631
Assembly Challenges and Demonstrations of Ultra-large Antenna in Package for Automotive Radar Applications	635
Investigation on Package Warpage and Reliability of the large size 2.5D Molded Interposer on Substrate (MIoS) Package	. 643
Characterizations and Challenges of Adhesion Promotion Solutions for HSIO Package Development Yi Yang (Intel Corporation, USA), Marcel Wall (Intel Corporation, USA), Rengarajan Shanmugam (Intel Corporation, USA), Sarah Wozny (Intel Corporation, USA), Xin Yan (Intel Corporation, USA), Mohit Khurana (Intel Corporation, USA), Rajeev Ranjan (Intel Corporation, USA), Dilan Seneviratne (Intel Corporation, USA), Kassandra Nikkhah (Intel Corporation, USA), and Suddhasattwa Nad (Intel Corporation, USA)	. 648

Tai Chong Chai (Institute of Microelectronics, A*STAR, Singapore), Soon Wee Ho (Institute of Microelectronics, A*STAR, Singapore), Ser Choong Chong (Institute of Microelectronics, A*STAR, Singapore), Sharon PS Lim (Institute of Microelectronics, A*STAR, Singapore), and Bhattcharya Surya (Institute of Microelectronics, A*STAR, Singapore)	655
Split-Fabric: A Novel Wafer-Scale Hardware Obfuscation Methodology using Silicon Interconnect Fabric Yousef Safari (McGill University, Canada), Yu-Tao Yang (University California, USA), Subramanian S. Iyer (University of California, USA), Toshifumi Nakatani (Maxentric Technologies LLC, USA), Neal Levine (Defense Microelectronics Activity, USA), and Boris Vaisband (McGill University, Canada)	660
A Self-Aligned Structure based on V-groove for Accurate Silicon Bridge Placement	668
Session 16: Hybrid & Direct Bonding Innovation, Optimization & Yield Improvement	<u>k</u>
The Wafer Bonding Yield Improvement through Control of SiCN Film Composition and Cu Pad Shape	674
Shape	

A Holistic Development Platform for Hybrid Bonding	91
Low Temperature Fine-pitch Cu-Cu Bonding Using Au Nanoparticles as Intermediate	'01
Wet Atomic Layer Etching of Copper Structures for Highly Scaled Copper Hybrid Bonding and Fully Aligned Vias	'07
A Study on Bonding Pad Structure and Layout for Fine Pitch Hybrid Bonding	'12

Session 17: Novel Characterization Techniques and Test Methods

QFN (Quad Flat No-lead) SAC Solder Joints Under Thermal Cycling: Identification of Two Failure Mechanisms	716
Tracking in-die Mechanical Stress through Silicon Embedded Sensors for Advanced Packaging Applications	
Damage Evolution of Double-Sided Copper Conductor on Multi-layer Flexible Substrate Under Bending	
Investigation of Stress Generated by Interconnection Processes with Micro-Raman Spectroscopy (µRS)	739
Development and Application of the Moisture-Dependent Viscoelastic Model of Polyimide in Hygro-Thermo-Mechanical Analysis of fan-out Interconnect	746
A Novel Quantitative Adhesion Measurement Method for Thin Polymer and Metal Layers for Microelectronic Applications	754

Session 18: Flexible, Wearable Sensors and Electronics

Andrew Stemmermann (SunRay Scientific, Inc., USA), Dan Balder (SunRay	762
Scientific, Inc., USA), Madhu Stémmermann (SunRay Scientific, Inc, USA), Christopher Tabor (Air Force Research Laboratory, USA), Nancy Stoffel (GE Research, USA), Riadh Al-Haidari (Binghampton University, USA), Behnam Garakani (Binghampton University, USA), Udara Somarathna El Medhi Abbara (Binghampton University, USA), Mohammed Alhendi (Binghampton University, USA), and Mark Poliks (Binghampton University, USA)	
Wireless Nanomembrane Electronics and Soft Packaging Technologies for Noninvasive, Real-Time Monitoring of Muscle Activities	'69
Modeling of Spreading Behavior of UV-Curable Dielectric Ink from Its Rheological Characteristics	74
Sujie Kang (Mechatronics Research, Samsung Electronics, Republic of Korea), Jung Shin Lee (Mechatronics Research, Samsung Electronics, Republic of Korea), Jung Woo Cho (Mechatronics Research, Samsung Electronics, Republic of Korea), Sun Woo Park (Mechatronics Research, Samsung Electronics, Republic of Korea), Seungdon Lee (Mechatronics Research, Samsung Electronics, Republic of Korea), Hyunjin Lee (Mechatronics Research, Samsung Electronics, Republic of Korea), and Daniel Minwoo Rhee (Mechatronics Research, Samsung Electronics, Republic of Korea)	
Fabrication of Flexible Li-ion Battery Electrodes Using "Battlets" Approach with Ionic Liquid Electrolyte for Powering Wearable Devices	'80
Smart Biofeedback Earbud Achieved by SiP with 3D Composite Polymer Package	'86
Current Carrying Capacity of Inkjet-Printed Nano-Silver Interconnects on Mesoporous PET Substrate	⁷ 94
El Mehdi Abbara (State University of New York, USA), Gurvinder Singh Khinda (State University of New York, USA), Mohammed Alhendi (State University of New York, USA), Riadh Alhaidari (State University of New York, USA), Firas Alshatnawi (State University of New York, USA), Behnam Garakani (State University of New York, USA), Udara S. Somarathna (State University of New York, USA), and Mark D. Poliks (State University of New York, USA)	J4

Session 19: Advances in Fan-Out Panel Level Packaging

Tanja Braun (Fraunhofer Institute for Reliability and Microintegration, Germany), Ole Hölck (Fraunhofer Institute for Reliability and Microintegration, Germany), Mattis Obst (Fraunhofer Institute for Reliability and Microintegration, Germany), Steve Voges (Fraunhofer Institute for Reliability and Microintegration, Germany), Ruben Kahle (Fraunhofer Institute for Reliability and Microintegration, Germany), Lars Böttcher (Fraunhofer Institute for Reliability and Microintegration, Germany), Mathilde Billaud (Fraunhofer Institute for Reliability and Microintegration, Germany), Lutz Stobbe (Fraunhofer Institute for Reliability and Microintegration, Germany), Karl-Friedrich Becker (Fraunhofer Institute for Reliability and Microintegration, Germany), Rolf Aschenbrenner (Fraunhofer Institute for Reliability and Microintegration, Germany), Marcus Voitel (Technical University Berlin, Germany), Friedrich-Leonhard Schein (Technical University Berlin, Germany), Lutz Gerholt (Technical University Berlin, Germany), and Martin Schneider Bamplow (Technical University Berlin, Germany), and Martin Schneider-Ramelow (Technical University Berlin, Germany) Da-Hee Kim (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Jae-Ean Lee (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Gyujin Choi (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Sunguk Lee (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Giho Jeong (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Hongwon Kim (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), Seokwon Lee (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea), and Dong Wook Kim (Test & System Package (TSP) Samsung Electronics Co., Ltd, South Korea)

A Hybrid Panel Level Package (Hybrid PLP) Technology Based on a 650-mm \times 650-mm Platform . 824	
Eoin O´Toole (Amkor Technology Vila do Conde, Portugal), José Luís Silva (Amkor Technology Vila do Conde, Portugal), Filipe Cardoso (Amkor Technology Vila do Conde, Portugal), José Silva (Amkor Technology Vila do Conde, Portugal), Luís Alves (Amkor Technology Vila do Conde, Portugal), Márcio Souto (Amkor Technology Vila do Conde, Portugal), Nuno Delduque (Amkor Technology Vila do Conde, Portugal), Aníbal Coelho (Amkor Technology Vila do Conde, Portugal), José Míguel Silva (Amkor Technology Vila do Conde, Portugal), WonChul Do (Amkor Technology Incheon, Korea), and JinYoung Khim (Amkor Technology Incheon, Korea)	
Package Reliability Evaluation of 600mm FOPLP with 6-Sided Die Protection with 0.35mm Ball Pitch	8
Panel-Based Large-Scale RDL Interposer Fabricated using 2-µm-Pitch Semi-Additive Process for Chiplet-Based Integration	6
Harnessing the power of 4nm silicon with Gen 2 M-Series™ Fan-out and Adaptive Patterning® providing ultra-high-density 20µm device bond pad pitch	.5
All Copper Is Not Created Equal — Examples of Grain Engineering In Plating	1

Session 20: Enhancements in Fine-Pitch Interconnects, Redistribution Layers and Through-Vias

A study of Failure Mechanism in the Formation of Fine RDL Patterns and Vias for Heterogeneous Packages in Chip Last Fan-out Panel Level Packaging	856
Novel Plasma Process for Build-up Film in the Fine Wiring Fabrication	. 862
Fine Copper Lines with High Adhesion on High Rigidity Dielectrics	867
Fabrication and Characterization of Nanoporous Gold (NPG) Interconnects for Wafer Level Packaging	873
Role of (111) Nanotwinned Cu on Dissolution Behavior and Interfacial Reaction in Micro-scale Nanotwinned Cu/Sn/Ni Interconnects	883
Approaches for a Solely Electroless Metallization of Through-Glass Vias	889
Atmospheric HF Vapor Based Silicon Etching with Pt Catalyst for high Fidelity through Silicon via (TSV) Fabrication	898

Session 21: Millimeter-Wave RF Components and Modules for 5G

Metaconductor Based Highly Energy Efficient Differential Striplines for 112 Gbps Data Bus with Sub 0.1 dB/mm Package Insertion Loss	3
Multi-terminal Ultra-thin 3D Nanoporous Silicon Capacitor Technology for High-Speed Circuits Decoupling	3
Mechanical and Ka-Band Electrical Reliability Testing of Interconnects in 5G Wearable System-on-Package Designs Under Bending	1
X-band Passive Circuits Using 3-D Printed Hollow Substrate Integrated Waveguides	1
A Novel Simulation Methodology Reflecting System Power Scenario using a Markov-Chain-Based Stochastic Random Power Model)
Towards Mass Production of Air Filled Substrate Integrated Waveguides (AFSIW) for Ultra-low Loss, Broadband Radar Applications	7

Characterisation of RF Connectors and Components for Advanced 5G Applications	342
Session 22: AI, Quantum Computing and Novel 3D Packaging Solutions	
RF Characterization on Nb-Based Superconducting Silicon Interconnect Fabric for Future Large Scale Quantum Applications	949
Development of Cu-Cu Side-by-Side Interconnection using Controlled Electroless Cu Plating S. Y. A. Chen (National Taiwan University, Taiwan), P. S. Shih (National Taiwan University, Taiwan), F. L. Chang (National Taiwan University, Taiwan), S. J. Gräfner (National Taiwan University, Taiwan), J. H. Huang (National Taiwan University, Taiwan), C. H. Huang (National Taiwan University, Taiwan), C. R. Kao (National Taiwan University, Taiwan), Y. S. Lin (ASE Group, Taiwan), Y. C. Hung (ASE Group, Taiwan), C. L. Kao (ASE Group, Taiwan), and D. Tarng (ASE Group, Taiwan)	956
Design of Compact Microwave Multiplexer for RF Reflectometry Characterization of Silicon-Based Spin Qubits	962
Small Package Size Low Power CMOS Image Sensor using Two Different Type Small Through Silicon Vias Technology for 3D Packaging	967
Stability Analysis of Nanoscale Copper-Carbon Hybrid Interconnects Bhawana Kumari (Indian Institute of Technology (Indian School of Mines, India), Rohit Sharma (Indian Institute of Technology Ropar, India), and Manodipan Sahoo (Indian Institute of Technology (Indian School of Mines), India)	972

Functional Testing of AI Cores through Thinned 3D I/O Buffer Dies in 3D Die-Stacked Modules	977
Mukta Farooq (IBM Research), Arvind Kumar (IBM Research), Sae-Kyu Lee (IBM Research), Ravi Bonam (IBM Research), Juan-Manuel Gomez (IBM Research), James Kelly (IBM Research), Kohji Hosokawa (IBM Research), Akiyo Nomura (IBM Research), Yasuteru Kohda (IBM Research), Timothy Dickson (IBM Research), Katsuyuki Sakuma (IBM Research), Hiroyuki Mori (IBM Research), Joshua Rubin (IBM Research), Iqbal Saraf (IBM Research), Vinay Pai (IBM Research), Pablo Nieves (IBM Research), Yandong Li (IBM Research), Abraham DelaPena (IBM Research), Thomas Wassick (IBM Systems), Eric Perfecto (IBM Research), Christopher Carr (IBM Research), Viraj Sardesai (IBM Research), Eric Miller (IBM Research), Jennifer Oakley (IBM Research), Spyridon Skordas (IBM Research), Sean Teehan (IBM Research), Dale McHerron (IBM Research), Jeff Burns (IBM Research), and Rama Divakaruni (IBM Research)	,,,,
Exploring the Impact of Parametric Variability on Eye Diagram of On-chip Multi-walled Carbon Nanotube Interconnects using Fast Machine Learning Techniques	981
Demonstration of Flexible Encapsulation in Assembly Industry	987
Pretreatment and Structuring of Spatial Circuit Carriers Based on Alumina for High Temperatures and High Frequencies	992

	Dµm Pitch Bumping of Singulated Die using a Temporary Metal-Embedded Chip Assembly focess
	Souheil Nadri (HRL Laboratories, LLC, USA), B-A. Clayton Tu (HRL Laboratories, LLC, USA), Florian Herrault (HRL Laboratories, LLC, USA), Courtney Wilt (HRL Laboratories, LLC, USA), Partia Naghibi (HRL Laboratories, LLC, USA), Marko Pavlov (HRL Laboratories, LLC, USA), Joel Wong (HRL Laboratories, LLC, USA), and Phan Vu (HRL Laboratories, LLC, USA)
	ealization of High A/R and Fine Pitch Cu Pillars Incorporating High Speed Electroplating ith Novel Strip Process
Н	igh Density Thin Film Flex Technology for Advanced Packaging Applications
	Oomm Full Thickness Si-Based IC Singulation Using Plasma Dicing for Advanced Packaging echnologies
In	vestigation of LowK WLCSP Die Strength Impact Induced by Singulation Process

Session 24: Thermal Management and Warpage Analysis of Highly Integrated Packages

Thermal Challenges and Design Considerations in Heterogeneous Integrated Through-Silicon-Interposer Platform for III-V HEMT Flip Chip
Assessment of Thermal-aware Floorplans in a 3D IC for Server Applications
Effect of Storage on Reliability of Thin-Flexible Laminated and Unlaminated Batteries in Wearable Applications
Modeling and Design for System-Level Reliability and Warpage Mitigation of Large 2.5D Glass BGA Packages
Effective Computational Models for Addressing Asymmetric Warping of Fan-Out Reconstituted Wafer Packaging

Warpage and RDL Stress Analysis in Large Fan-Out Package with Multi-Chiplet Integration ... 1074 Jen-Hsien Wong (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), NanYi Wu (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Wei-Hong Lai (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Dao-Long Chen (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Tang-Yuan Chen (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Chung-Hao Chen (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Yi-Hsien Wu (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Yung-Shun Chang (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Chin-Li Kao (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), David Tarng (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), Teck Chong Lee (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)), and Cp Hung (Corporate R&D Center, Advanced Semiconductor Engineering Inc., Taiwan (R.O.C)) The Optimal Solution of Fan-Out Embedded Bridge (FO-EB) Package Evaluation During the Vito Lin (Cooperate R & D, Siliconware Precision Industries Co. Ltd.Taiwan), David Lai (Cooperate R & D, Siliconware Precision

Session 25: Advancements in 2.5D and 3D Packaging Technology

Industries Co. Ltd. Taiwan), and Yu-Po Wang (Cooperate R & D,

Siliconware Precision Industries Co. Ltd.Taiwan)

S R L L L	Performance and Energy Efficient Computing with Advanced SolCTM Scaling
S (/ (/	stigation of Moisture-Induced Warpage of Chip-on-Wafer in 2.5D IC Package
R A II S E	Packaging for Heterogeneous Integration
5μm (α (π (π Ε (α (α (α (α (α (α (α (α (α (α (α (α (α	Temperature Backside Damascene Processing on Temporary Carrier Wafer Targeting 7µm and in pitch microbumps for N Equal and Greater than 2 Die to Wafer TCB Stacking
Perf S S	nonstration of Glass-based 3D Package Architectures with Embedded Dies for High Formance Computing
Ju (2 (2 (2 (2 (2 (2 (2 (2 (2 (2 (2 (2 (2	Stacking Process Investigation by Soldering Bonding Technology

Session 26: Soldered and Sintered Interconnections

Novel Ag Salt Paste for Large Area Cu-Cu Bonding in Low Temperature Low Pressure and Air Condition	1126
Condition Chuantong Chen (Osaka University, Japan), Bowen Zhang (Osaka University, Japan), Katsuaki Suganuma (Osaka University, Japan), and Takuya Sekiguchi (Central Research Center, TOPPAN FORMS CO., LTD, Japan)	
Bonding Properties of Cu Paste in Low Temperature Pressureless Processes	1133
Tight-Pitched 10 µm-Width Solder Joints for c-2-c and c-2-w 3D-Integrtion in NCF Environment Murugesan Mariappan (Tohoku University, Japan), Shizu Fukuzumi (Showa Denko Materials Co., Ltd., Japan), Tomoaki Shibata (Showa Denko Materials Co., Ltd., Japan), Hiroyuki Hashimoto (Tohoku University, Japan), JiChel Bea (Tohoku University, Japan), Mitsumasa Koyanagi (T-Micro, Japan), and Takafumi Fukushima (Tohoku Univesity, Japan)	1138
Influence of Micro Voids in Flip Chip Bump on Electro-Migration Reliability	1144
Study of Failure and Microstructural Evolution in SAC Solder Interconnects Induced by AC Electromigration Condition Yi Ram Kim (University of Texas at Arlington, USA), Allison T. Osmanson (University of Texas at Arlington, USA), Choong-Un Kim (University of Texas at Arlington, USA), Patrick F. Thompson (Texas Instruments, Inc., USA), and Qiao Chen (Texas Instruments, Inc., USA)	1153
A Study on Warpage and Reflow Profile for Extreme Extension of Mass Reflow Bonding Jiwon Shin (Package Process Development Team, South Korea), Kwangbok Woo (Package Process Development Team, South Korea), Donguk Kwon (Package Process Development Team, South Korea), Youngja Kim (Package Process Development Team, South Korea), Youngmin Lee (Package Process Development Team, South Korea), Dongwoo Kang (Package Process Development Team, South Korea), Krutikesh Sahoo (Integration and Performance Scaling, USA), Haoxiang Ren (Integration and Performance Scaling, USA), Yu-Pei Huang (Integration and Performance Scaling, USA), Ujash Shah (Integration and Performance Scaling, USA), Yutao Yang (Integration and Performance Scaling, USA), Ankit Kuchhangi (Integration and Performance Scaling, USA), and Subramanian Iyer (Integration and Performance Scaling, USA)	1158

Low Temperature Formation of SAC-SnBi BGA Interconnections using Solid Liquid Inter-Diffusion (SLID)	63
Session 27: Interconnection Reliability	
Process-Reliability Relationships of SnBiAg and SnIn Solders for Component Attachment on Flexible Direct-Write Additive Circuits in Wearable Applications	72
Interconnection Reliability of Mini LEDs for Display Applications	84
Study of Long-Term Solder Joint and Board-Level Reliability Performance of Thin Nickel Plating ENEPIG Laminate LGA Package	92
Thermal Cycling Induced Interconnect Stability Degradation Mechanism in Low Melting Temperature Solder Joints	99
Fabrication and Reliability Analysis of Quasi-Single Crystalline Cu Joints using Highly <111>-Oriented Nanotwinned Cu	06

A Comparative Study of the Thermomechanical Reliability of Fully-Filled and Conformal Through-Glass Via
Broadband Characterization of Polymers under Reliability Stresses and Impact of Capping Layer
Nicolas Pantano (imec Leuven, Belgium), Emmanuel Chery (imec Leuven, Belgium), Maaike Op de Beeck (imec Ghent, Belgium), John Slabbekoorn (imec Leuven, Belgium), and Eric Beyne (imec Leuven, Belgium)
Session 28: Packaging Assembly: Solder, Sintering, and Thermal Interface Materials
High Thermal Graphite TIM Solution Applied to Fan-Out Platform
Optimizing Reflowed Solder TIM (sTIMs) Processes for Emerging Heterogeneous Integrated Packages
Large, High Conductivity Direct-Fill Copper Thermal Vias for High Power Devices
Vacuum Fluxless Reflow Technology for Fine Pitch First Level Interconnect Bumping Applications

Thermal Performance of Advanced TIMs for High-Power FCLBGAs YoungJoon Koh (Amkor technology Korea, Inc., Republic of Korea), SangHyuk Kim (Amkor technology Korea, Inc., Republic of Korea), EunSook Sohn (Amkor technology Korea, Inc., Republic of Korea), and JinYoung Khim (Amkor technology Korea, Inc., Republic of Korea)
Non-oil Bleed Thermal gap Fillers for Long-Term Reliability of Solid State Drive
Printed Silver Micro-Pillars Embedded in a Phase Change Material Matrix for Thermal Management Applications
Session 29: Materials and Processes for Fan-Out and Advanced Packaging
High Fluorescence Photosensitive Materials for AOI Inspection of Fan-Out Panel Level Package
Selective Epoxy Mold Compound Slurry for Advanced Packaging Technology
Laser Direct Structuring of Semiconductor Liquid Encapsulants for Active Mold Packaging 1277 Chunlin He (Henkel Corporation, USA), Ruud deWit (Henkel Corporation, USA), Jay Chao (Henkel Corporation, USA), Tim Champagne (Henkel Corporation, USA), Rose Guino (Henkel Corporation, USA), Tony Winster (Henkel Corporation, USA), Ramachandran Trichur (Henkel Corporation, USA), Mario Saliba (Henkel Corporation, USA), Frank Song (Henkel Corporation, USA), Florian Roick (LPKF Laser & Electronics AG, Germany), Simon Heitmann (LPKF Laser & Electronics AG, Germany), Bernd Roesener (LPKF Laser & Electronics AG, Germany), and Johan Stelling (LPKF Laser & Electronics AG, Germany)

Large-Scale Production of Boron Nitride Nanosheets-Based Epoxy Nanocomposites with Ultrahigh Through-Plane Thermal Conductivity for Electronic Encapsulation	2
Photonic Debond: Scalability and Advancements	7
A Novel Method of Low Temperature, Pressureless Interconnection for Wafer Level Scale 3D Packaging	4
Cracking-Less Heat-Resistant Electroless Ni-P Plating Film for Wide Bandgap Power Modules 1300 Ming-chun Hsieh (Osaka University, Japan), Chuantong Chen (Osaka University, Japan), Aiji Suetake (Osaka University, Japan), Zheng Zhang (Osaka University, Japan), Katsuaki Suganuma (Osaka University, Japan), Ryuji Saito (Okuno Chemical Industries Co., Ltd., Japan), Norihiko Hasegawa (Okuno Chemical Industries Co., Ltd., Japan), Kei Hashizume (Okuno Chemical Industries Co., Ltd., Japan), and Kuniaki Otsuka (Okuno Chemical Industries Co., Ltd., Japan)	

Session 30: High-Speed Challenges in Power and Signal Integrity

Integration of Foundry MIM Capacitor and OSAT Fan-Out RDL for High Performance RF Filters 1310 Pao-Nan Lee (Advanced Semiconductor Engineering (ASE), Inc., Taiwan), Yu-Chang Hsieh (Advanced Semiconductor Engineering (ASE), Inc., Taiwan), Hung-Lun Lo (WIN Semiconductors Corp., Taiwan), Chang-Ho Li (WIN Semiconductors Corp., Taiwan), Fan-Hsiu Huang (WIN Semiconductors Corp., Taiwan), James Lin (WIN Semiconductors Corp., Taiwan), Wei-Chu Hsu (Advanced Semiconductor Engineering (ASE), Inc., Taiwan), and Chen-Chao Wang (Advanced Semiconductor Engineering (ASE), Inc., Taiwan)	
Optimization of 2.5D Organic Interposer Channel for Die and Chiplets	5
Reference Clock Assessment Techniques for PCIe Gen5 and Beyond	3
Co-Design and Signal-Power Integrity/EMI Co-Analysis of a Switchable High-Speed Inter-Chiplet Serial Link on an Active Interposer	•
Fast Channel Analysis and Design Approach using Deep Learning Algorithm for 112Gbs HSI Signal Routing Optimization	7

Mercy Daniel-Aguebor (Georgia Institute of Technology, USA), Mutee Ur Rehman (Georgia Institute of Technology, USA), Serhat Erdogan (Georgia Institute of Technology, USA), Kyoung-Sik Moon (Georgia Institute of Technology, USA), Nikita Ambasana (Georgia Institute of Technology), Saibal Mukhopadhyay (Georgia Institute of Technology, USA), Madhavan Swaminathan (Georgia Institute of Technology, USA), Liang Yuan Dai (Columbia University), Keren Bergman (Columbia University, USA), Daniel Jang (Columbia Univerity, USA), and Mingoo Soek (Columbia University, USA)	
Session 31: Fan-Out Packaging Technologies and Applications	
Fan-out Wafer Level Package for Memory Applications Ho-Young Son (SK Hynix Inc., Republic of Korea), Ki-Jun Sung (SK Hynix Inc., Republic of Korea), Bok-Kyu Choi (SK Hynix Inc., Republic of Korea), Jong-Hoon Kim (SK Hynix Inc., Republic of Korea), and Kangwook Lee (SK Hynix Inc., Republic of Korea)	1349
Substrate Silicon Wafer Integrated Fan-out Technology (S-SWIFT®) Packaging with Fine Pitch Embedded Trace RDL SangHyun Jin (R&D, Amkor Technology Korea, Inc., Republic of Korea), WonChul Do (R&D, Amkor Technology Korea, Inc., Republic of Korea), JinSuk Jeong (R&D, Amkor Technology Korea, Inc.), HyunGoo Cha (R&D, Amkor Technology Korea, Inc., Republic of Korea), YunKyung Jeong (R&D, Amkor Technology Korea, Inc., Republic of Korea), and JinYoung Khim (R&D, Amkor Technology Korea, Inc., Republic of Korea)	1355
Advanced Fanout Packaging Technology for Hybrid Substrate Integration	1362
Advanced Chip Last Process Integration for Fan Out WLP	1371

Package Design and Measurements for Radar Emulator using Accelerators and Photonics \dots 1342

Hsiang-Yao Hsiao (Institute of Microelectronics, A*STAR, Singapore), Boon Long Lau (Institute of Microelectronics, A*STAR, Singapore), Pei Siang Lim (Institute of Microelectronics, A*STAR, Singapore), Teck Guan Lim (Institute of Microelectronics, A*STAR, Singapore), and Tai Chong Chai (Institute of Microelectronics, A*STAR, Singapore)	
Chip-Last FOWLP Based Antenna-in-Package (FO-AiP) for 5G mmWave Application	:4
A Heterogeneously Integrated and Flexible Inorganic Micro-display on FlexTrateTM using Fan-Out Wafer-Level Packaging	0
Session 32: Advanced Interconnect and Wire Bond Technologies	
for Flexible Device Applications	
)5
for Flexible Device Applications Infrared Curing of Flip Chip Electrically Conductive Adhesive (ECA) Interconnections)5
for Flexible Device Applications Infrared Curing of Flip Chip Electrically Conductive Adhesive (ECA) Interconnections	
Infrared Curing of Flip Chip Electrically Conductive Adhesive (ECA) Interconnections	

Foils and the Effect of Intermediate Electroless Cu Layers	1413
Evaluation of an Anisotropic Conductive Epoxy for Interconnecting Highly Stretchable Conductors to Various Surfaces Riadh Al-Haidari (Center for Advanced Microelectronics Manufacturing (CAMM), State University of New York at Binghamton), Behnam Garakani (Center for Advanced Microelectronics Manufacturing (CAMM), State University of New York at Binghamton), Mohammed Alhendi (Center for Advanced Microelectronics Manufacturing (CAMM), State University of New York at Binghamton), Udara S. Somarathna (enter for Advanced Microelectronics Manufacturing (CAMM), State University of New York at Binghamton), Mark D. Poliks (Center for Advanced Microelectronics Manufacturing (CAMM), State University of New York at Binghamton), Christopher E. Tabor (Air Force Research Laboratory (AFRL), Michelle Yuen (Air Force Research Laboratory (AFRL); National Academies of Science Fellow), Madhu Stemmermann (SunRay Scientific), and Nancy Stoffel (General Electric Global Research)	1422
Laser Soldered Wire Bonding on Liquid Printed and Sputtered Contact Structures on Thin-Flexes and Injection Molded Devices	1430
Cu/Co Metaconductor Based Highly Energy-Efficient Bonding Wires for next Generation Millimeter wave Electronic Interconnects	1442

Session 33: Advanced Reliability Modeling and Characterization

the Assembly to Use in the Field	ŀ6
Reliability Challenges of High-Density Fan-out Packaging for High-Performance Computing Applications	4
A Comprehensive Study of Crack Initiation and Delamination Propagation at the Cu/Polyimide Interface in Fan-out Wafer Level Package During Reflow Process	9
Observation of Fatigue and Creep Ratcheting Failure in Solder Joints Under Pulsed Direct Current Electromigration Testing	5
Evolution of SAC305 Mechanical Behavior Due to Damage Accumulation During Cycling 147 Mohammad Ashraful Haq (Auburn University, USA), Mohd Aminul Hoque (Auburn University, USA), Golam Rakib Mazumder (Auburn University, USA), Jeffrey C. Suhling (Auburn University, USA), and Pradeep Lall (Auburn University, USA)	2
Board-Level Solder Joint Reliability of QFN Packages with Enclosure and Placement Effects in Various Form Factors	2

Shape Dependency of Fatigue Life in Solder Joints of Chip Resistors	489
Session 34: Processing Enhancements in Fan-Out and Heterogeneous Integration	
Optimization of Temporary Carrier Technology for HDFO Packaging	495
Optimization of PI & PBO Layers Lithography Process for High Density Fan-OUT Wafer Level Packaging & Next Generation Heterogeneous Integration Applications Employing Digitally Driven Maskless Lithography	500
Analysis of Pattern Distortion by Panel Deformation and Addressing it by using Extremely Large Exposure Field Fine-Resolution Lithography	505
Solutions to Overcome Warpage and Voiding Challenges in Fanout Wafer-level Packaging 1 Vidya Jayaram (Intel Corporation, USA), Vipul Mehta (Intel Corporation, USA), Yiqun Bai (Intel Corporation, USA), and John C Decker (Intel Corporation, USA)	511
Dry Etch Processing in Fan-Out Panel-Level Packaging — An Application for High-Density Vertical Interconnects and Beyond	518

Fabrication, Characterization and Electromechanical Reliability of Stretchable Circuitry for Health Monitoring Systems	24
Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration	31
Session 35: Packaging with Additive Manufacturing for Harsh Conditions	
High Temperature Die Interconnection Approaches Firas Alshatnawi (Binghamton University, USA), Mohammed Alhendi (Binghamton University, USA), Riadh A. Al-Haidari (Binghamton University, USA), Rajesh S. Sivasubramony (Binghamton University, USA), El Mehdi Abbara (Binghamton University, USA), K Udara Somarathna (Binghamton University, USA), Mark D. Poliks (Binghamton University, USA), Peter Borgesen (Binghamton University, USA), David M. Shaddock (GE Research Center, One Research Circle, USA), Nancy Stoffel (GE Research Center, One Research Circle, USA), and Cathleen Hoel (GE Research Center, One Research Circle, USA)	39
3D Cryogenic Interposer for Quantum Computing Application	46
Flexible Metamaterial Lens for Magnetic Field and Signal-to-Noise Ratio Improvements in 1.5 T and 3 T Magnetic Resonance Imaging	51

Self-healing of Interconnect Cracks for Reliable and Defect-Free Smart Manufacturing of Flexible Packages
Akeeb Yunus Hassan (Florida International University, USA), Reshmi Banerjee (Florida International University, USA), Asahi Tomitaka (University of Houston-Victoria, USA), and Markondeya Raj Pulugurtha (Florida International University, USA)
Additively Manufactured RF GRIN Lenses for Highly Directive Low Power Transmitters 1562 Jonathon H. Copley (United States Naval Academy, USA), Hatem ElBidWeihy (United States Naval Academy, USA), Connor S. Smith (United States Naval Academy, USA), Christopher R. Milligan (Department of Defense, USA), and Nam Nicholas Mai (Department of Defense, USA)
A Low Profile Two-Phase Immersion Cooling Stack-up Based on Detachable Boiling Enhancement Layer on Lidded Electronic Packages
Ultraprecise Deposition of Micrometer-Size Conductive Features for Advanced Packaging 1573 Aneta Wiatrowska (XTPL SA, Poland), Piotr Kowalczewski (XTPL SA, Poland), Karolina Fiączyk (XTPL SA, Poland), Łukasz Witczak (XTPL SA, Poland), Jolanta Gadzalińska (XTPL SA, Poland), Mateusz Łysień (XTPL SA, Poland), Ludovic Schneider (XTPL SA, Poland), Łukasz Kosior (XTPL SA, Poland), and Filip Granek (XTPL SA, Poland)
Session 36: Modeling and Characterization of Interfaces and Interconnects
Sustained High Temperature Fracture Toughness Evolution of Chip-UF and Substrate-UF nterfaces in FCBGAs for Automotive Applications
Sustained High Temperature Fracture Toughness Evolution of Chip-UF and Substrate-UF nterfaces in FCBGAs for Automotive Applications
Sustained High Temperature Fracture Toughness Evolution of Chip-UF and Substrate-UF Interfaces in FCBGAs for Automotive Applications

Singapore), Yeow Chon Ong (Micron Semiconductor Asia Operations Pte. Ltd, Singapore), Hong Wan Ng (Micron Semiconductor Asia Operations Pte. Ltd, Singapore), Ling Pan (Micron Semiconductor Asia Operations Pte. Ltd, Singapore), Christopher Glancey (Micron Technology, Inc., USA), Koustav Sinha (Micron Technology, Inc., USA), and Richard Fan (Micron Memory Taiwan Co., Ltd, Taiwan)	. 1608
An Extensive Simulation Study of the Interfacial Delamination in Molded Underfill Flip-Chip Packages by Finite Element Method Based on Virtual Crack Closure Technique Guang-Chao Lyu (South China University of Technology, China; Guangdong Provincial Engineering Technology R&D Center of Electronic Packaging Materials and Reliability, China), Hong-Guang Wang (South China University of Technology, China; Guangdong Provincial Engineering Technology R&D Center of Electronic Packaging Materials and Reliability, China), Min-Bo Zhou (South China University of Technology, China; Guangdong Provincial Engineering Technology R&D Center of Electronic Packaging Materials and Reliability, China), and Xin-Ping Zhang (South China University of Technology, China; Guangdong Provincial Engineering Technology R&D Center of Electronic Packaging Materials and Reliability, China)	1614
Mechanical Simulation and Modeling for Reliability of 6-in-1 Power Module	1624
Session 37: Interactive Presentations 1	
The Effect of Thermal Stress on the Reliability of all-Printed Vias on Flexible Substrates Udara S. Somarathna (The State University of New York at Binghamton,	1629
USA), Mohammed Alhendi (The State University of New York at Binghamton, USA), Behnam Garakani (The State University of New York at Binghamton, USA), Behnam Garakani (The State University of New York at Binghamton, USA), Mark D. Poliks (The State University of New York at Binghamton, USA), Darshana L. Weerawarne (University of Colombo, Sri Lanka), Joseph Iannotti (GE Global Research, USA), Christopher J. Kapusta (GE Global Research, USA), Nancy Stoffel (GE Global Research, USA), and Stephen G. Gonya (Lockheed Martin, USA)	
USA), Mohammed Alhendi (The State University of New York at Binghamton, USA), Behnam Garakani (The State University of New York at Binghamton, USA), Mark D. Poliks (The State University of New York at Binghamton, USA), Darshana L. Weerawarne (University of Colombo, Sri Lanka), Joseph Iannotti (GE Global Research, USA), Christopher J. Kapusta (GE Global Research, USA), Nancy Stoffel (GE Global Research, USA), and Stephen G. Gonya (Lockheed Martin, USA) Mechanical Property Evolution in SAC+Bi Lead-Free Solders Subjected to Various Thermal Exposure Profiles	.1637
USA), Mohammed Alhendi (The State University of New York at Binghamton, USA), Behnam Garakani (The State University of New York at Binghamton, USA), Mark D. Poliks (The State University of New York at Binghamton, USA), Darshana L. Weerawarne (University of Colombo, Sri Lanka), Joseph Iannotti (GE Global Research, USA), Christopher J. Kapusta (GE Global Research, USA), Nancy Stoffel (GE Global Research, USA), and Stephen G. Gonya (Lockheed Martin, USA) Mechanical Property Evolution in SAC+Bi Lead-Free Solders Subjected to Various Thermal Exposure Profiles	. 1637

Effects of β-Sn Crystal Orientation on the Deformation Behavior of SAC305 Solder Joints 1658 Debabrata Mondal (Auburn University, USA), Mohammad Ashraful Haq (Auburn University, USA), Jeffrey C. Suhling (Auburn University, USA), and Pradeep Lall (Auburn University, USA)	
Reconstructing more Sinterable Surfaces for Copper Nanoparticles to Form High-Strength Cu-Cu Joints in Air Atmosphere	
Two-/Multi-photon Imaging for Characterization of Fine Line Features and Microvias in Advanced Packaging	
Development of Advanced Liquid Cooling Solution on Data Centre Cooling	
The Effects of Bi Doping and Aging on Viscoplasticity of Sn-Ag-Cu-Bi alloys	

Numerical Simulation of Cu/Polymer-Dielectric Hybrid Bonding Process Using Finite Element Analysis	5
Sasi Kumar Tippabhotla (Institute of Microelectronics, A*STAR (Agency for Science, Technology, and Research), Singapore), Ji Lin (Institute of Microelectronics, A*STAR (Agency for Science, Technology, and Research), Singapore), and Han Yong (Institute of Microelectronics, A*STAR (Agency for Science, Technology, and Research), Singapore)	
Investigating Moisture Diffusion in Mold Compounds (MCs) for Fan-Out-Wafer-Level-Packaging (FOWLP)	4
Mechanical and Thermal Characterization Analysis of Chip-Last Fan-out Chip on Substrate 171 Wei-Jie Yin (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), Wei-Hong Lai (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), Ying-Xu Lu (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), KarenYU Chen (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), Hung-Hsien Huang (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), Tang-Yuan Chen (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), Chin-Li Kao (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC)), and Cp Hung (Advanced Semiconductor Engineering (ASE) Inc., Taiwan (ROC))	1
Low Cost Copper Based Sintered Interconnect Material for Optoelectronics Packaging	0

Anisotropy of Curing Residual Stress of Underfill in the Encapsulation Under Three-Dimensionally Constrained Condition Based on in-Situ Characterization	1726
Materials, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China)	
Study of Small Polyimide Open Size in Contact Resistance and Reliability for Flip Chip Cu Pillar Package	. 1732
Package Design trough Reliable Predictive Modeling and Its Validation	1738
Block Thermal Model for High Power Lidded Packages	. 1745
Thermo-Mechanical Reworkable Epoxy Underfill in Board-Level Package: Material Characteristics and Reliability Criteria	. 1750

A Parameter Study for the Design Optimization to Relieve Pattern Stress of PCB Under the Temperature Cycling Condition	1754
Characterization and Design Improvement of a High Bandwidth, High Frequency Flexible Connector for Signal Delivery	1759
Investigation of Reflow Effect and Empirical Lifetime Modeling on the Board Level Solder Joint Reliability Kwangwon Seo (Samsung Electronics, Korea), Keunho Rhew (Samsung Electronics, Korea), Choongpyo Jeon (Samsung Electronics, Korea), Youngsung Choi (Samsung Electronics, Korea), Jinsoo Bae (Samsung Electronics, Korea), Yuchul Hwang (Samsung Electronics, Korea), Hoosung Kim (Samsung Electronics, Korea), and Sangwoo Pae (Samsung Electronics, Korea)	1764
Finite Element Influence Analysis of Power Module Design Options Marius van Dijk (Fraunhofer Institute for Reliability and Microintegration IZM, Germany), Olaf Wittler (Fraunhofer Institute for Reliability and Microintegratrion IZM, Germany), Ping-Chi Hung (Universal Scientific Industrial Co., Ltd., Taiwan), Wei-Hong Lai (Advanced Semiconductor Engineering, Inc., Taiwan), Cheng-Yu Hsieh (Advanced Semiconductor Engineering, Inc., Taiwan), Thomas Wang (Advanced Semiconductor Engineering, Inc., Taiwan), and Martin Schneider-Ramelow (Technical University of Berlin, Germany)	1770
Solder Joint Fatigue Studies Subjected to Board-Level Random Vibration for Automotive Applications	1777
2-D Fluid Simulation Approach for Miniwave Soldering	1785

Component Level Reliability Evaluation of Low Cost 6-Sided Die Protection Versus Wafer Level Chip Scale Packaging with 350um Ball Pitch Jacinta Aman Lim (nepes Corporation), Byung-Cheol Kim (nepes Corporation), Rizi Valencia-Gacho (nepes Corporation), and Brett Dunlap (nepes Corporation)	1791
Simulation of the Filler Stuck Mechanism in Molding Process and Verification Tzu Chieh Chien (Central Development Engineering(CDE), ASE Group, Taiwan), Shih Kun Lo (Central Development Engineering(CDE), ASE Group, Taiwan), Yen Hua Kuo (Central Development Engineering(CDE), ASE Group, Taiwan), Hui Chung Liu (Central Development Engineering(CDE), ASE Group, Taiwan), Zong Yuan Li (Central Development Engineering(CDE), ASE Group, Taiwan), Yi Nong Lin (Central Development Engineering(CDE), ASE Group, Taiwan), Lu Ming Lai (Central Development Engineering(CDE), ASE Group, Taiwan), and Kuang Hsiung Chen (Central Development Engineering(CDE), ASE Group, Taiwan)	1798
Inlet/outlet Induced Failures During flip-Chip Bonding of Large area Chip with Embedded Microchannels Jianyu Du (China University of Geosciences (Beijing), China; Peking University, China), Yuchi Yang (Peking University, China), Huaiqiang Yu (26th Research Institute of China Electronics Technology Group Corporation, China), Han Xu (Peking University, China), Deyin Zheng (Peking University, China), Qi Wang (Peking University, China), Jiajie Kang (China University of Geosciences (Beijing), China), and Wei Wang (Peking University, China) Session 38: Interactive Presentations 2	1805
Multi-layer Chips on Wafer Stacking Technologies with Carbon Nano-Tubes as Through-Silicor Vias and Its Potential Applications for Power-Via Technologies	n 1811
A De-embedding and Embedding Procedure for High-Speed Channel Eye Diagram Oscilloscop Measurement	-
Physics-Based Nested-ANN Approach for Fan-Out Wafer-Level Package Reliability Prediction . 1827 Peilun Yao (Hong Kong University of Science and Technology, China), Jun Yang (Hong Kong University of Science and Technology, China), Yonglin Zhang (Hong Kong University of Science and Technology, China), Xiaoshun Fan (Hong Kong University of Science and Technology, China), Haibin Chen (Hong Kong University of Science and Technology, China), Jinglei Yang (Hong Kong University of Science and Technology, China), and Jingshen Wu (Smart Manufacturing Thrust, Systems Hub, Hong Kong	

A Fully Additive Approach for the Fabrication of Roghayeh Imani (EISLAB, Electrical, & Space En Technical University, Sweden), Sarthak Acharyo Space Engineering Luleå Technical University, S Chouhan (EISLAB, Electrical, & Space Engineeri University, Sweden), Jerker Delsing (EISLAB, Elec Engineering Luleå Technical University, Sweder (M3S Research group, University of Oulu, Finland	a (EISLAB, Electrical, & Sweden), Shailesh ng Luleå Technical ctrical, & Space n), and Sarthak Acharya
60 GHz 0-360° Passive Analog Delay Line in Liqu Conductor-Backed Fully-Enclosed Coplanar Way Jinfeng Li (Imperial College London, United King University, United Kingdom)	veguide 1841
Development of Smart Sensor Array Mat for Re Ruiqi Lim (Institute of Microelectronics, Singap Sikkandhar (Institute of Microelectronics, Singapore Cheng (Institute of Microelectronics, Singapore	apore), and Ming-Yuan
Modeling and Mitigating Fiber Weave Effect using Method	
Die Floorplan and PKG Design Impacts on Power a Single Power Domain	
System Level Power Supply Induced Jitter Suppl Links	
Team, Samsung Electronics, Korea)	, , ,

System-Level Verification of a Packaged Silicon Photonics-Based Transceiver	75
A Novel Frequency Mixing Based Beam-Steering Phased Array for K-Band Applications 18 Yu Ping Liu (Oakland University, USA) and Amanpreet Kaur (Oakland University, USA)	82
Automated Detection and Segmentation of HBMs in 3D X-ray Images using Semi-Supervised Detection Learning	-
New Packaging Technology for Disruptive 1- and 2-Dimensional VCSEL Arrays and Their Electro-Optical Performance and Applications	198
Electrospray Printing of Polyimide Films for Electronics Packaging Applications	06
Addressing 5G NR Filter Challenges with Hybrid Technologies	114
Hybrid Lithography Approach for Single Mode Polymeric Waveguides and Out-of-Plane Couplin Mirrors	_

Performance of Flexible Microwave Antenna Under Environmental Stress Emuobosan Enakerakpo (Center for Advanced Microelectronics Manufacturing (CAMM), Binghamton University, USA), Ashraf I Umar (Center for Advanced Microelectronics Manufacturing (CAMM), Binghamton University, Binghamton, USA), Mohammed Alhendi (Center for Advanced Micro electronics manufacturing (CAMM), Binghamton University, Binghamton, USA), Dylan Richmond (Center for Advanced Microelectronic Manufacturing (CAMM), Binghamton University, Binghamton, USA), Mark D. Poliks (Center for Advanced Microelectronic Manufacturing (CAMM), Binghamton University, Binghamton, USA), Tom Rovere (Lockheed Martin, Owego, USA), and Stephen Gonya (Lockheed Martin, Owego, USA)	1927
TSV-less Power Delivery for Wafer-scale Assemblies and Interposers Haoxiang Ren (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), Saptadeep Pal (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), Guangqi Ouyang (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), Randall Irwin (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), Yu-Tao Yang (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA), and Subramanian S. Iyer (Center for Heterogeneous Integration and Performance Scaling (CHIPS), UCLA, USA)	1934
Modeling the Effect of Trace Profiles on the RF Performance of Additively Manufactured Microstrip Transmission Lines on Polyimide Substrates	1940
Modeling the Effect of Surface Roughness for Screen-Printed Silver ink on Flexible Substrates	1946
A Broadband High-Efficiency Charge Pump for Ambient RF Energy Harvesting — Powering Underground RFID Based Sensors	1952
Modeling of Adaptive Receiver Performance using Generative Adversarial Networks	1958

Session 39: Interactive Presentations 3

The Investigation of dry Plasma Technology in each Steps for the Fabrication of High Performance Redistribution Layer	64
Chip Last Fanout Chip on Substrate (FOCoS) Solution for Chiplets Integration	70
Die to Wafer Hybrid Bonding for Chiplet and Heterogeneous Integration: Die Size Effects Evaluation-Small Die Applications	75
Yield Improvement in Chip to Wafer Hybrid Bonding	82
Study of Parameter Tuning for the Curing Condition on ABF Type for Large FCBGA Package . 198 Rick Ye (Siliconware Precision Industries Co. Ltd, Taiwan (R.O.C.)), Eric Chen (Siliconware Precision Industries Co. Ltd, Taiwan (R.O.C.)), Wen-Yu Teng (Siliconware Precision Industries Co. Ltd, Taiwan (R.O.C.)), Andrew Kang (Siliconware Precision Industries Co. Ltd, Taiwan (R.O.C.)), and Yu-Po Wang (Siliconware Precision Industries Co. Ltd, Taiwan (R.O.C.))	87
Next Gen Laser Assisted Bonding (LAB) Technology	91
Swelling Analysis of Negative-Tone Photosensitive Dielectric Materials for Fine Pitch Redistribution Layers	96

RF Characterization in Range of 18GHz in Fan-out Package Structure Molded by Epoxy McCompound with EMI Shielding Property	_
Plasma Chamber Environment Control to Enhance Bonding Strength for Wafer-to-Wafer Processing	Bonding 2008
Study of Large Exposure Field Lithography for Advanced Chiplet Packaging	2013
Epoxy Resin with Metal Complex Additives for Improved Reliability of Epoxy-Copper Joint Jiaxiong Li (Georgia Institute of Technology, USA), John Wilson (Georgia Institute of Technology, USA), Dylan Cheung (Georgia Institute of Technology, USA), Zhijian Sun (Georgia Institute of Technology, USA), Kyoung-Sik Moon (Georgia Institute of Technology, USA), Madhavan Swaminathan (Georgia Institute of Technology, USA), and Ching-Ping Wong (Georgia Institute of Technology, USA)	2018
Wirebonding Based 3-D SiC IC Stacks for High Temperature Applications	2023
Electrical Design and Modeling of Silicon Carbide Power Modules for Inverter Applications Vignesh Shanmugam Bhaskar (Institute Of Microelectronics, Singapore), Jong Ming Chinq (Institute Of Microelectronics, Singapore), Kazunori Yamamoto (Institute Of Microelectronics, Singapore), and Gongyue Tang (Institute Of Microelectronics, Singapore)	s 2028
Reliability of Component Attachment using ECA and LTS on Flexible Additively Printed Ink-Jet Circuits for Signal-Filtering in Wearable Applications	2033
Micro-Spray with Silver ink for Maskless Selective-Area EMI Shielding Kisu Joo (Ntrium Incorporation, Korea), Kyu Jae Lee (Ntrium Incorporation, Korea), Jung Yoon Moon (Ntrium Incorporation, Korea), Yoon-Hyun Kim (Ntrium Incorporation, Korea), Jinhwan Chung (Ntrium Incorporation, Korea), Se Young Jeong (Ntrium Incorporation, Korea), and Seung Jae Lee (Ntrium Incorporation, Korea)	N/A

Embedded-IC Package using Si-Interposer for mmWave Applications
Carrier Systems for Collective Die-to-Wafer Bonding
Superb Sinterability of the Cu Paste Consisting of Bimodal Size Distribution Cu Nanoparticles for Low-Temperature and Pressureless Sintering of Large-Area Die Attachment and the Sintering Mechanism
Reliability of Ag Bonding Wires and its Coated Variants from the Perspective of IMC Degradation and Its Correlation to wire and Epoxy Molding Compound Material Properties Under Corrosive Environment
Design and Simulation to Reduce the Crosstalk of Ultra-Fine Line Width/Space in the Redistribution Layer
Influence of Tribo-Mechanical Characteristics of Advanced EN Coating for Electronic Packaging Housing

Analysis on Optimal Chip Floorplanning Considering Various Types of Decoupling Capacitors in Package PDN	91
Novel Polymer Design for Ultra-low Stress Dielectrics	95
Session 40: Interactive Presentations 4	
Ultra-High Conductivity Interconnects for 77K CMOS Using Heterogeneous Integration 20 Golam Sabbir (University of California, Los Angeles) and Subramanian S. Iyer (University of California, Los Angeles)	99
Functional Demonstration of < 0.4-pJ/bit, 9.8 µm Fine-Pitch Dielet-to-Dielet Links for Advanced Packaging using Silicon Interconnect Fabric	04
Integration of High Performance GaN LEDs for Communication Systems and Smart Society . 21 Zeinab Shaban (Tyndall National Institute, University College Cork, Ireland), Mehrdad Saei (Tyndall National Institute, University College Cork, Ireland), Brian Corbett (Tyndall National Institute, University College Cork, Ireland), and Zhi Li (Tyndall National Institute, University College Cork, Ireland)	11
Low Temperature Metal-to-Metal Direct Bonding in Atmosphere using Highly (111) Oriented Nanotwinned Silver Interconnects	16
Scalable Through Molding Interconnection realization for advanced Fan Out Wafer Level Packaging applications	22

A Hybrid Bonding Interconnection with a Novel Low-Temperature Bonding Polymer System 2' Yu Min Lin (Industrial Technology Research Institute (ITRI), Taiwan), Po-Chih Chang (Industrial Technology Research Institute (ITRI), Taiwan), Ou-Hsiang Lee (Industrial Technology Research Institute (ITRI), Taiwan), Wei-Lan Chiu (Industrial Technology Research Institute (ITRI), Taiwan), Tao-Chih Chang (Industrial Technology Research Institute (ITRI), Taiwan), Hsiang-Hung Chang (Industrial Technology Research Institute (ITRI), Taiwan), Chia-Hsin Lee (Brewer Science, Taiwan; National Yang Ming Chiao Tung University), Baron Huang (Brewer Science, Taiwan), Mei Dong (Brewer Science, Taiwan), Duo Tsai (Brewer Science, Taiwan), Chang-Chun Lee (National Tsing Hua University, Taiwan), and Kuan-Neng Chen (National Yang Ming Chiao Tung University, Taiwan)	128
Chiplets Integrated Solution with FO-EB Package in HPC and Networking Application	135
Signal Integrity Design and Analysis with Link Budget Results of HBM2E Module on Latest High Density Organic Laminate	141
Effect of Isothermal Aging on Properties of In-48Sn and In-Sn-8Cu Alloys	148
Ag die-Attach Paste Modified by WC Additive for high-Temperature Stability Enhancement 2 Yang Liu (Osaka University, Japan), Chuantong Chen (Osaka University, Japan), Katsuaki Suganuma (Osaka University, Japan), Takeshi Sakamoto (Daicel Corporation, Japan), Minoru Ueshima (Daicel Corporation, Japan), Takuya Naoe (Osaka University, Japan), and Hiroshi Nishikawa (Osaka University, Japan)	153
PSI Design Solutions for High Speed Die-to-Die Interface in Chiplet Applications	158
Thermal Compression Cu-Cu Bonding using Electroless Cu and the Evolution of Voids Within Bonding Interface	163

Novel Zero Side-Etch Process for <1 µm Package Redistribution Layers	. 2168
MaxQFP: A High Density QFP	. 2174
Printed Microwave Connector Jotham Kasule (University of Massachusetts Lowell, USA), Shokat Ganjeheizadeh Rohani (University of Massachusetts Lowell, USA), Mark Pothier (University of Massachusetts Lowell, USA), Yuri Piro (University of Massachusetts Lowell, USA), Alkim Akyurtlu (University of Massachusetts Lowell, USA), and Craig Armiento (University of Massachusetts Lowell, USA)	. 2184
Creep and Microstructure Evolutions in SAC305 Lead Free Solder Subjected to Different Thermal Exposure Profiles	. 2191
Modeling of Cu-Cu Thermal Compression Bonding	. 2201
Mechanical Properties and Microstructures of Cu/In-48Sn Alloy/Cu with low Temperature TI Bonding	
Novel Pressure-Assist Silver Sintering Paste for SiC Power Device Attachment on Lead Frame Based Package	

Modeling High-Frequency and DC Path of Embedded Discrete Capacitor Connected by Double-Side Terminals with Multi-layered Organic Substrate and RDL-based Fan-out Package 2217
Heeseok Lee (Samsung Electronics, Co. Ltd., Korea), Kyojin Hwang (Samsung Electronics, Co. Ltd., Korea), Henry Kwon (Samsung Electronics, Co. Ltd., Korea), Jisoo Hwang (Samsung Electronics, Co. Ltd., Korea), Junso Pak (Samsung Electronics, Co. Ltd., Korea), and Ju Yeon Choi (Samsung Electronics, Co. Ltd., Korea)
Characterization of Low Loss Dielectric Materials for High-Speed and High-Frequency Applications
Evaluation on Bonding Reliability of SAC305/Sn-57.5Bi-0.4Ag BGA Solder Joints with Drop Impact test
High Throughput Void-Free Soldering with Pneumatic Reflow Method in Lead-Free Solder Die Attach
Influence of Prepreg Material Properties on Printed Circuit Board (PCB) Stack-up
Session 41: Student Interactive Presentations
Machine Learning Assisted Counterfeit IC Detection through Non-destructive Infrared (IR) Spectroscopy Material Characterization

ie-Attachment in Power Device Packaging	6
martphone App-Enabled Flex sEMG Patch Using FOWLP	3
Deep Learning Approach for Reflow Profile Prediction	9

11.4
Heterogeneous Integrated Packaging
Guolin Zhao (Central South University, China), Yuanyuan Yang (Shenzhen
Institute of Advanced Electronic Materials Shenzhen Institute of
Advanced Technology, CAS, China), Xiaohui Peng (Shenzhen Institute of
Advanced Electronic Materials Shenzhen Institute of Advanced
Technology, CAS, China), Houya Wu (Shenzhen Institute of Advanced
Electronic Materials Shenzhen Institute of Advanced Technology, CAS,
China), Haoliang Lin (Shenzhen Institute of Advanced Electronic
Materials Shenzhen Institute of Advanced Technology, CAS, China), Gang
Li (Shenzhen Institute of Advanced Electronic Materials Shenzhen
Institute of Advanced Technology, CAS, China), Pengli Zhu (Shenzhen
Institute of Advanced Electronic Materials Shenzhen Institute of
Advanced Technology, CAS, China), Rong Sun (Shenzhen Institute of
Advanced Electronic Materials Shenzhen Institute of Advanced
Technology, CAS, China), Chingping Wong (Georgia Institute of
Technology, USA), and Wenhui Zhu (Central South University, China)
Demonstration and Comparison of Vertical Via-less Interconnects in Laminated Glass Panels
from 40-170 GHz
Lakshmi Narasimha Vijay Kumar (Georgia Institute of Technology, USA),
Kyoung-Sik Moon (Georgia Institute of Technology, USA), Madhavan
Swaminathan (Georgia Institute of Technology, USA), Kimiyuki Kanno
(JSR Corporation, Japan), Hirokazu Ito (JSR Corporation, Japan), Taku
Ogawa (JSR Corporation, Japan), and Koichi Hasegawa (JSR Corporation,
Japan)
Monte Carlo Particle Simulation of Avalanche Breakdown in a Reverse Biased Diode with Full
Monte Carlo Particle Simulation of Avalanche Breakdown in a Reverse Biased Diode with Full Band Structure
Band Structure228
Band Structure

Novel Sn–Cu Based Composite Solder Preforms Capable of Low Temperature Reflow for Die Attachment of High Temperature Power Electronics and the Transient Liquid Phase Bonding Process
Ru-Zeng Shi (South China University of Technology, China), Min-Bo Zhou (South China University of Technology, China), and Xin-Ping Zhang (South China University of Technology, China)
Trust Validation of Chiplets using a Physical Inspection based Certification Authority
Security Challenges of MEMS Devices in HI Packaging
Influence of Height Difference Between Chip and Substrate on RDL in Silicon-Based Fan-OUT Package
Symmetric-Cell EBG Theory and Its Applications to Vias Daisy Chain for Residual Stub Detection
Millimeter-Wave Antenna Design and Performance Analysis for Automotive Applications 2339 Mohammad Shahed Pervez (Oakland University, USA), Amanpreet Kaur (Oakland University, USA), and Md Mamun Ur Rashid (Oakland University, USA)

Author Index