

2022 IEEE Custom Integrated Circuits Conference (CICC 2022)

**Newport Beach, California, USA
24-27 April 2022**



**IEEE Catalog Number: CFP22CIC-POD
ISBN: 978-1-7281-8280-3**

**Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP22CIC-POD
ISBN (Print-On-Demand):	978-1-7281-8280-3
ISBN (Online):	978-1-6654-0756-4
ISSN:	0886-5930

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

SESSION 3: IMAGING FOR HEALTH AND AUTOMOTIVE SYSTEMS

A Review of Silicon Photonics LiDAR.....	1
<i>Hossein Hashemi</i>	
Solid-State dToF LiDAR System Using an Eight-Channel Addressable, 20W/Ch Transmitter, and a 128–128 SPAD Receiver with SNR-Based Pixel Binning and Resolution Upscaling	9
<i>Shenglong Zhuo, Lei Zhao, Tao Xia, Lei Wang, Shi Shi, Yifan Wu, Chang Liu, Chill Wang, Yuwei Wang, Yuan Li, Hengwei Yu, Jiqing Xu, Aaron Wang, Zhihong Lin, Yun Chen, Rui Bai, Xuefeng Chen, Patrick Yin Chiang</i>	
A 13.1mm ² 512 × 256 Multimodal CMOS Array for Spatiochemical Imaging of Bacterial Biofilms	11
<i>Kangping Hu, Joseph Incandela, Xiaoyu Lian, Joseph W. Larkin, Jacob K. Rosenstein</i>	
A 36×40 Wireless Fluorescence Image Sensor for Real-Time Microscopy in Cancer Therapy	13
<i>Rozhan Rabbani, Hossein Najafiaghdam, Biqi Zhao, Megan Zeng, Vladimir Stojanovic, Rikky Muller, Mekhail Anwar</i>	

SESSION 4: POWER MANAGEMENT DIRECTIONS

Piezoelectric-Based Power Conversion: Recent Progress, Opportunities, and Challenges	15
<i>Jessica D. Boles, Joshua J. Piel, Elaine Ng, Joseph E. Bonavia, Jeffrey H. Lang, David J. Perreault</i>	
An 86.7%-Efficient Three-Level Boost Converter with Active Voltage Balancing for Thermoelectric Energy Harvesting.....	23
<i>Loan Pham-Nguyen, Nam Nguyen-Dac, Thinh Tran-Dinh, Hieu Minh Pham, Minkyu Je, Sang-Gug Lee, Hanh-Phuc Le</i>	
A 93.7%-Efficiency 5-Ratio Switched-Photovoltaic DC-DC Converter.....	25
<i>Sandeep Reddy Kukunuru, Loai G. Salem</i>	
A 400-to-12 V Fully Integrated Switched-Capacitor DC-DC Converter Achieving 119 mW/mm ² at 63.6 % Efficiency	27
<i>Tuur Van Daele, Filip Tavernier</i>	

SESSION 5: MM-WAVE TRANSCEIVERS AND SYSTEMS

A 23–37GHz Autonomous Two-Dimensional MIMO Receiver Array with Rapid Full-FoV Spatial Filtering for Unknown Interference Suppression	29
<i>Boce Lin, Tzu-Yuan Huang, Amr Ahmed, Min-Yu Huang, Hua Wang</i>	
IC and Array Technologies for 100–300GHz Wireless.....	31
<i>M. J. W. Rodwell, Ali A. Farid, A. S. H. Ahmed, M. Seo, U. Soyulu, A. Alizadeh, N. Hosseinzadeh</i>	
A 220 GHz Sliding-IF Quadrature Transmitter with 38-DB Conversion Gain and 8-DBm P _{sat} in 0.13-Mm SiGe BiCMOS	36
<i>Zekun Li, Jixin Chen, Jiayang Yu, Huanbo Li, Zichun Zheng, Rui Zhou, Peigen Zhou, Zhe Chen, Wei Hong</i>	

A 3.8-DB NF, 23-40GHz Phased-Array Receiver with 14-Bit Phase & Gain Manager and Calibration-Free Dual-Mode 28-52dB Image Rejection Ratio for 5G NR.....	38
<i>Zhixian Deng, Huizhen Jenny Qian, Changxuan Han, Yifan Li, Xun Luo</i>	

SESSION 7: COMPUTING-IN-MEMORY

Comprehending In-Memory Computing Trends Via Proper Benchmarking	40
<i>Naresh R. Shanbhag, Saion K. Roy</i>	
5GHz SRAM for High-Performance Compute Platform in 5nm CMOS	47
<i>R. Mathur, M. Kumar, V. Asthana, S. Aggarwal, S. Gupta, D. Wanjul, A. Baradia, S. Thota, P. Jain, B. Zheng, A. Cubeta, S. Thyagarajan, A. Chen, Y. Chong</i>	
An Area-Efficient 6T-SRAM Based Compute-In-Memory Architecture with Reconfigurable SAR ADCs for Energy-Efficient Deep Neural Networks in Edge ML Applications.....	49
<i>Avishek Biswas, Hetul Sanghvi, Mahesh Mehendale, G. Preet</i>	
A 915–1220 TOPS/W Hybrid In-Memory Computing Based Image Restoration and Region Proposal Integrated Circuit for Neuromorphic Vision Sensors in 65nm CMOS.....	51
<i>Xueyong Zhang, Arindam Basu</i>	
A 177 TOPS/W, Capacitor-Based In-Memory Computing SRAM Macro with Stepwise-Charging/Discharging DACs and Sparsity-Optimized Bitcells for 4-Bit Deep Convolutional Neural Networks	53
<i>Bo Zhang, Jyotishman Saikia, Jian Meng, Dewei Wang, Soonwan Kwon, Sungmeen Myung, Hyunsoo Kim, Sang Joon Kim, Jae-Sun Seo, Mingoo Seok</i>	
DCT-RAM: A Driver-Free Process-In-Memory 8T SRAM Macro with Multi-Bit Charge-Domain Computation and Time-Domain Quantization	55
<i>Zhiyu Chen, Qing Jin, Zhanghao Yu, Yanzhi Wang, Kaiyuan Yang</i>	
A 133.6TOPS/W Compute-In-Memory SRAM Macro with Fully Parallel One-Step Multi-Bit Computation	57
<i>Edward Choi, Injun Choi, Chanhee Jeon, Gichan Yun, Donghyeon Yi, Sohmyung Ha, Ik-Joon Chang, Minkyu Je</i>	
T-PIM: A 2.21-to-161.08TOPS/W Processing-In-Memory Accelerator for End-To-End On-Device Training	59
<i>Jaehoon Heo, Junsoo Kim, Wontak Han, Sukbin Lim, Joo-Young Kim</i>	

SESSION 8: SMART SENSORS FOR THE IOT, WEARABLES, AND IMPLANTABLES

Smart Threads for Tissue-Embedded Bioelectronics	61
<i>Sameer Sonkusale</i>	
Wireless Frequency-Division Multiplexed 3D Magnetic Localization for Low Power Sub-Mm Precision Capsule Endoscopy.....	68
<i>Michella Rustom, Constantine Sideris</i>	
A Battery-Less Crystal-Less 49.8 μ W Neural-Recording Chip Featuring Two-Tone RF Power Harvesting	70
<i>Ziyi Chang, Changgui Yang, Yunshan Zhang, Zhuhao Li, Tianyu Zheng, Yuxuan Luo, Shaomin Zhang, Kedi Xu, Yong Chen, Gang Pan, Bo Zhao</i>	

Wireless, Batteryless, and Secure Implantable System-On-A-Chip for 1.37mmHg Strain Sensing with Bandwidth Reconfigurability for Cross-Tissue Adaptation	72
<i>M. R. Abdelhamid, U. Ha, U. Banerjee, F. Adib, A. Chandrakasan</i>	
A 0.8V/0.6V 2.2 μ W Time-Domain Analog Front-End with 540mVpp Input Range, 81.6dB SNDR and 80M Ω Input Impedance	74
<i>Liheng Liu, Tianxiang Qu, Pengjie Wang, Yao Zhang, Zhiliang Hong, Jiawei Xu</i>	
An Energy-Harvesting Stamp-Sized Reader for Distance-Immune Interrogation of Passive Wireless Sensors	76
<i>Siavash Kananian, Cheng Chen, Ada S. Y. Poon</i>	

SESSION 9: SYSTEM FOUNDATIONS FOR INTELLIGENT COMPUTING

StreamGCN: Accelerating Graph Convolutional Networks with Streaming Processing	78
<i>Atefeh Sohrabizadeh, Yuze Chi, Jason Cong</i>	
An Energy-Efficient and Runtime-Reconfigurable FPGA-Based Accelerator for Robotic Localization Systems	86
<i>Qiang Liu, Zishen Wan, Bo Yu, Weizhuang Liu, Shaoshan Liu, Arijit Raychowdhury</i>	
A 39pJ/Label 1920–1080 165.7 FPS Block PatchMatch Based Stereo Matching Processor on FPGA	88
<i>Hongyu Wang, Wei Zhou, Xiangyu Zhang, Xin Lou</i>	
Hardware/Software Co-Design for Neuromorphic Systems	90
<i>Rajit Manohar</i>	
The Rise of SoC FPAA Devices	95
<i>Jennifer Hasler</i>	

SESSION 10: ADVANCED TRANSMITTER & RECEIVER CIRCUITS

A Phase-Modulation Phase-Shifting Phased-Array Transmitter with 10-Bit Fast-Locking Phase Self-Calibration and 0/2.5/6/12dB Power Back-Offs Efficiency Enhancement	103
<i>Jie Zhou, Huizhen Jenny Qian, Bingzheng Yang, Yiyang Shu, Xun Luo</i>	
A 1-to-4GHz Multi-Mode Digital Transmitter in 40nm CMOS Supporting 200MHz 1024-QAM OFDM Signals with More than 23dBm/66% Peak Power/Drain Efficiency	105
<i>Mohammadreza Beikmirza, Yiyu Shen, Leo C. N. De Vreede, Morteza S. Alavi</i>	
Watt-Level Triple-Mode Quadrature SFCPA with 56 Peaks for Ultra-Deep PBO Efficiency Enhancement Using IQ Intrinsic Interaction and Adaptive Phase Compensation	107
<i>Bingzheng Yang, Huizhen Jenny Qian, Yiyang Shu, Jie Zhou, Xun Luo</i>	
22–30GHz Quadrature Hybrid SCPA with LO Leakage Self-Suppression and Distributed Parasitic-Cancelling Sub-PA Array for Linearity and Efficiency Enhancement	109
<i>Bingzheng Yang, Huizhen Jenny Qian, Yiyang Shu, Jie Zhou, Xun Luo</i>	
A Compact Wideband Joint Bidirectional Class-G Digital Doherty Switched-Capacitor Transmitter and N-Path Quadrature Receiver Through Capacitor Bank Sharing	111
<i>Jeongseok Lee, Doohwan Jung, David Munzer, Hua Wang</i>	

A 0.5–3GHz Receiver with a Parallel Preselect Filter Achieving 120dB/dec Channel Selectivity and +28dBm Out-Of-Band IIP3	113
<i>M. A. Montazerolghaem, Leo C. N. De Vreede, Masoud Babaie</i>	
A 2GHz Voltage Mode Power Scalable RF-Front-End with 2.5dB-NF and 0.5dBm-1dBCP	115
<i>Justin Yonghui Kim, Antonio Liscidini</i>	

SESSION 13: ADVANCED TECHNOLOGIES & SECURITY

System Technology Co-Optimization and Design Challenges for 3D IC	117
<i>Supreet Jeloka, Brian Cline, Shidhartha Das, Benoit Labbe, Alejandro Rico, Rainer Herberholz, Javier Delacruz, Rahul Mathur, Shawn Hung</i>	
TICA: A 0.3V, Variation-Resilient 64-Stage Deeply-Pipelined Bitcoin Mining Core with Timing Slack Inference and Clock Frequency Adaption	123
<i>Jieyu Li, Weifeng He, Bo Zhang, Guanghui He, Jun Yang, Mingoo Seok</i>	
A 334uW 0.158mm ² Saber Learning with Rounding Based Post-Quantum Crypto Accelerator.....	125
<i>Archisman Ghosh, J. M. B. Mera, Angshuman Karmakar, Debayan Das, Santosh Ghosh, Ingrid Verbauwhede, Shreyas Sen</i>	
PVT Tolerant Zero Bit-Error-Rate Physical Unclonable Function Exploiting Hot Carrier Injection Aging in 7nm FinFET Technology	127
<i>Jyothi Bhaskar Velamala, Siang-Jih Sean Wu, Padma Penmatsa, Kuan-Yueh James Shen, David Johnston, Rachael Parker</i>	
A Lossless and Modeling Attack-Resistant Strong PUF with <4E-8 Bit Error Rate.....	129
<i>Yan He, Qixuan Yu, Kaiyuan Yang</i>	
3nm Gate-All-Around (GAA) Design-Technology Co-Optimization (DTCO) for Succeeding PPA by Technology.....	131
<i>Taejoong Song, Hakchul Jung, Giyoung Yang, Hoyoung Tang, Hayoung Kim, Dongwook Seo, Hoonki Kim, Woojin Rim, Sanghoon Baek, Sangyeop Baeck, Jonghoon Jung</i>	
A Digital Cascoded Signature Attenuation Countermeasure with Intelligent Malicious Voltage Drop Attack Detector for EM/Power SCA Resilient Parallel AES-256.....	138
<i>Archisman Ghosh, Dong-Hyun Seo, Debayan Das, Santosh Ghosh, Shreyas Sen</i>	

SESSION 14: HIGH SPEED CIRCUITS AND SYSTEMS FOR ELECTRICAL AND OPTICAL

110-GHz-Bandwidth InP-HBT AMUX/ADEMUX Circuits for Beyond-1-Tb/s/ch Digital Coherent Optical Transceivers.....	140
<i>Munehiko Nagatani, Hitoshi Wakita, Teruo Jyo, Tsutomu Takeya, Hiroshi Yamazaki, Yoshihiro Ogiso, Miwa Mutoh, Yuta Shiratori, Minoru Ida, Fukutaro Hamaoka, Masanori Nakamura, Takayuki Kobayashi, Hiroyuki Takahashi, Yutaka Miyamoto</i>	
A 112 Gb/s –8.2 dBm Sensitivity 4-PAM Linear TIA in 16nm CMOS with Co-Packaged Photodiodes	148
<i>Dhruv Patel, Alireza Sharif-Bakhtiar, Anthony Chan Carusone</i>	
A 10/2.5-Gb/s Hyper-Supplied CMOS Low-Noise Burst-Mode TIA with Loud Burst Protection and Gearbox Automatic Offset Cancellation for XGS-PON.....	150
<i>Chen Tan, Wei Huang, Yonghui Fan, Jing Li, Chuanhao Yu, Wenbo Shi, Shiti Huang, Zhenyu Yin, Chenfan Cao, Lei Jing, Zhixiong Ren, Xiaoyan Gui, Bing Zhang, Dan Li, Li Geng</i>	

Interconnect in the Era of 3DIC	152
<i>Shenggao Li, Mu-Shan Lin, Wei-Chih Chen, Chien-Chun Tsai, Cheng-Hsiang Hsieh</i>	
A 60-Gb/s/Pin Single-Ended PAM-4 Transmitter with Timing Skew Training and Low Power Data Encoding in Mimicked 10nm Class DRAM Process.....	157
<i>Joohwan Kim, Junyoung Park, Jindo Byun, Changkyu Seol, Chang Soo Yoon, Eunseok Shin, Hyunyoon Cho, Youngdo Um, Sucheol Lee, Hyungmin Jin, Kwangseob Shin, Hyunsub Norbert Rie, Minsu Jung, Jin-Hee Park, Go-Eun Cha, Minjae Lee, Youngmin Kim, Byeori Han, Yuseong Jeon, Jisun Lee, Hyejeong So, Sungduk Kim, Wansoo Park, Tae Young Kim, Youngdon Choi, Jung-Hwan Choi, Hyungjong Ko, Sang-Hyun Lee</i>	
A Jitter-Robust 40Gb/s ADC-Based Multicarrier Receiver Front End in 22nm FinFET	159
<i>Yuanming Zhu, Julian Camilo Gomez Diaz, Srujan Kumar Kaile, Il-Min Yi, Tong Liu, Sebastian Hoyos, Samuel Palermo</i>	

SESSION 15: HIGH-SPEED DATA CONVERTERS

A 48dB-SFDR, 43dB-SNDR, 50GS/s 9-Bit 2 \times -Interleaved Nyquist DAC in Intel 16	161
<i>Hariprasad Chandrakumar, Thomas W. Brown, Dimitri Frolov, Zinia Tuli, Iwen Huang, Said Rami</i>	
A 10b 700MS/s Single-Channel 1b/Cycle SAR ADC Using a Monotonic-Specific Feedback SAR Logic with Power-Delay-Optimized Unbalanced N/P-MOS Sizing	163
<i>Mingqiang Guo, Sai-Weng Sin, Liang Qi, Gangjun Xiao, Rui P. Martins</i>	
A 38GS/s 7b Time-Interleaved Pipelined-SAR ADC with Speed-Enhanced Bootstrapped Switch in 22nm FinFET	165
<i>Yuanming Zhu, Tong Liu, Srujan Kumar Kaile, Shiva Kiran, Il-Min Yi, Ruida Liu, Julian Camilo Gomez Diaz, Sebastian Hoyos, Samuel Palermo</i>	
A Calibration-Free 13b 625MS/s Tri-State Pipelined-SAR ADC with PVT-Insensitive Inverter-Based Residue Amplifier.....	167
<i>Xiaofeng Guo, Run Chen, Rongfeng Xu, Bin Li, Zhenqi Chen</i>	
High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range.....	169
<i>Shiyu Su, Mike Shuo-Wei Chen</i>	
A 30-MHz BW 74.6-DB SNDR 92-DB SFDR CT $\Delta\Sigma$ Modulator with Active Body-Bias DAC Calibration in 22nm FDSOI CMOS	177
<i>Marcel Runge, Julius Edler, Dario Schmock, Tobias Kaiser, Friedel Gerfers</i>	

SESSION 16: NEXT-GENERATION COMPUTING AND NEURAL INTERFACES

Spiking Neural Network Integrated Circuits: A Review of Trends and Future Directions	179
<i>Arindam Basu, Charlotte Frenkel, Lei Deng, Xueyong Zhang</i>	
An Analog Clock-Free Compute Fabric Base on Continuous-Time Dynamical System for Solving Combinatorial Optimization Problems.....	187
<i>Muya Chang, Xunzhao Yin, Zoltan Toroczkai, Xiaobo Hu, Arijit Raychowdhury</i>	
A 16-Channel 60 μ W Neural Synchrony Processor for Multi-Mode Phase-Locked Neurostimulation	189
<i>Uisub Shin, Cong Ding, Laxmeesha Somappa, Virginia Woods, Alik S. Widge, Mahsa Shoaran</i>	

A SAR-Assisted DC-Coupled Chopper-Stabilized 20 μ s-Artifact-Recovery $\Delta\Sigma$ ADC for Simultaneous Neural Recording and Stimulation.....	191
<i>Tania Moeinfard, Georg Zoidl, Hossein Kassiri</i>	
A 6.8 μ W AFE for Ear EEG Recording with Simultaneous Impedance Measurement for Motion Artifact Cancellation	193
<i>Aviral Pandey, Sina Faraji Alamouti, Justin Doong, Ryan Kaveh, Cem Yalcin, Mohammad Meraj Ghanbari, Rikky Muller</i>	
A 92%-Efficiency Inductor-Charging Switched-Capacitor Stimulation System with Level-Adaptive Duty Modulation and Offset Charge Balancing for Muscular Stimulation.....	195
<i>Kyeongho Eom, Han-Sol Lee, Minju Park, Seung Min Yang, Jong Chan Choe, Suk-Won Hwang, Young-Woo Suh, Hyung-Min Lee</i>	
A 65nm Implantable Gesture Classification SoC for Rehabilitation with Enhanced Data Compression and Encoding for Robust Neural Network Operation Under Wireless Power Condition.....	197
<i>Yijie Wei, Xi Chen, Jie Gu</i>	

SESSION 18: ANALOG TECHNIQUES

Photoplethysmography (PPG) Sensor Circuit Design Techniques.....	199
<i>Qiuyang Lin, Wim Sijbers, Christina Avidikou, Chris Van Hoof, Filip Tavernier, Nick Van Helleputte</i>	
A 1.8G Ω -Input-Impedance 0.15 μ V-Input-Referred-Ripple Chopper Amplifier with Local Positive Feedback and SAR-Assisted Ripple Reduction.....	207
<i>Tianxiang Qu, Qinjing Pan, Xiaoyang Zeng, Zhiliang Hong, Jiawei Xu</i>	
A Neural Recording Analog Front-End with Exponentially Tunable Pseudo Resistors and on-Chip Digital Frequency Calibration Loop Achieving 3.4% Deviation of High-Pass Cutoff Frequency in 5-to-500 Hz Range	209
<i>Renze Gan, Liangjian Lyu, Geng Mu, C. J. Richard Shi</i>	
Switched-Capacitor Circuits.....	211
<i>David J. Allstot, Un-Ku Moon, Gabor C. Temes</i>	
A 20 μ s Turn-On Time, 24kHz Resolution, 1.5–100MHz Digitally Programmable Temperature-Compensated Clock Generator with 7.5ppm/ $^{\circ}$ C Inaccuracy	219
<i>Yongxin Li, Nilanjan Pal, Tianyu Wang, Mostafa Gamal Ahmed, Ahmed Abdelrahman, Mohamed Badr Younis, Ruhao Xia, Kyu-Sang Park, Pavan Kumar Hanumolu</i>	
A 19–30ppm/ $^{\circ}$ C Temperature Coefficient Sub-Nanowatt CMOS Voltage Reference with 10-MA Sourcing Capability	221
<i>Hongchang Qiao, Chenchang Zhan</i>	
Filtering Trans-Impedance Amplifiers: From mW of Power to GHz of Bandwidth.....	223
<i>Nimesh Nadishka Miral, Karan Sohal, Danilo Manstretta, Rinaldo Castello</i>	

SESSION 19: HIGH PERFORMANCE DIGITAL

System-Level Design and Integration of a Prototype AR/VR Hardware Featuring a Custom Low-Power DNN Accelerator Chip in 7nm Technology for Codec Avatars.....	231
<i>H. Ekin Sumbul, Tony F. Wu, Yuecheng Li, Syed Shakib Sarwar, William Koven, Eli Murphy-Trotzky, Xingxing Cai, Elnaz Ansari, Daniel H. Morris, Huichu Liu, Doyun Kim, Edith Beigne</i>	

MPAM: Reliable, Low-Latency, Near-Threshold-Voltage Multi-Voltage/Frequency-Domain Network-On-Chip with Metastability Risk Prediction and Mitigation.....	239
<i>Chuxiong Lin, Weifeng He, Yannan Sun, Lin Shao, Bo Zhang, Jun Yang, Mingoo Seok</i>	
A 2.86Gb/s Fully-Flexible MU-MIMO Processor for Jointly Optimizing User Selection, Power Allocation, and Precoding in 28nm CMOS Technology	241
<i>Seungsik Moon, Namyoong Lee, Youngjoo Lee</i>	
An Energy-Efficient Cardiac Arrhythmia Classification Processor Using Heartbeat Difference Based Classification and Event-Driven Neural Network Computation with Adaptive Wake-Up.....	243
<i>J. Liu, J. Xiao, J. Fan, Q. Liu, Z. Zhu, S. Li, Z. Zhang, S. Yang, W. Shan, S. Lin, L. Chang, L. Zhou, J. Zhou</i>	
DDPMnet: All-Digital Pulse Density-Based DNN Architecture with 228 Gate Equivalents/MAC Unit, 28-TOPS/W and 1.5-TOPS/mm ² in 40nm.....	245
<i>Animesh Gupta, Viveka Konandur, Thoithoi Salam, Saurabh Jain, Orazio Aiello, Paolo Crovetto, Massimo Alioto</i>	
A 181 μ W Real-Time 3-D Hand Gesture Recognition System Based on Bi-Directional Convolution and Computing-Efficient Feature Clustering.....	247
<i>Yuncheng Lu, Zehao Li, Yuzong Chen, Tony Tae-Hyoung Kim</i>	
An 0.92 mJ/Frame High-Quality FHD Super-Resolution Mobile Accelerator SoC with Hybrid-Precision and Energy-Efficient Cache.....	249
<i>Zhiyong Li, Sangjin Kim, Dongseok Im, Donghyeon Han, Hoi-Jun Yoo</i>	

SESSION 20: FREQUENCY GENERATION TECHNIQUES

Recent Advances in High-Performance Frequency Synthesizer Design	251
<i>Salvatore Levantino</i>	
A 9GHz 72fs-Total-Integrated-Jitter Fractional-N Digital PLL with Calibrated Frequency Quadrupler.....	258
<i>Francesco Buccoleri, Simone M. Dartizio, Francesco Tesolin, Luca Avallone, Alessio Santiccioli, Agata Iesurum, Giovanni Steffan, Andrea Bevilacqua, Luca Bertulessi, Dmytro Cherniak, Carlo Samori, Andrea L. Lacaita, Salvatore Levantino</i>	
A 12.5-to-15.4GHz, -118.9dBc/Hz PN at 1MHz Offset, and 191.0dBc/Hz FoM VCO with Common-Mode Resonance Expansion and Simultaneous Differential 2ND-Harmonic Output Using a Single Three-Coil Transformer in 65nm CMOS	260
<i>Ruichang Ma, Haikun Jia, Wei Deng, Zhihua Wang, Baoyong Chi</i>	
A 2-GHz Dual-Path Sub-Sampling PLL with Ring VCO Phase Noise Suppression	262
<i>Yangtao Dong, Chirn Chye Boon, Kaituo Yang, Zhe Liu</i>	

SESSION 22: POWER CONVERTERS

Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators	264
<i>Zhaoqing Wang, Sung J. Kim, Keith Bowman, Mingoo Seok</i>	
A Single-Mode Dual-Path Buck-Boost Converter with Reduced Inductor Current Across All Duty Cases Achieving 95.58% Efficiency at 1A in Boost Operation	272
<i>Donghee Cho, Hyungjoo Cho, Sein Oh, Yoontae Jung, Sohmyung Ha, Chul Kim, Minkyu Je</i>	

A Fully In-Package 4-Phase Fixed-Frequency DAB Hysteretic Controlled DC-DC Converter with Enhanced Efficiency, Load Regulation and Transient Response	274
<i>Lei Zhao, Junyao Tang, Cheng Huang</i>	
A Hybrid Always-Dual-Path Recursive Step-Down Converter Using Adaptive Switching Level Control Achieving 95.4% Efficiency with 288mΩ Large-DCR Inductor	276
<i>Woojoong Jung, Minsu Kim, Hyunjun Park, Sungmin Yoo, Tae-Hwang Kong, Jun-Hyeok Yang, Michael Choi, Jongshin Shin, Hyung-Min Lee</i>	
A Highly-Integrated 20–300V 0.5W Active-Clamp Flyback DCDC Converter with 76.7% Peak Efficiency	278
<i>Christoph Rindfleisch, Jens Otten, Bernhard Wicht</i>	
A 0.66 W/mm ² Power Density, 92.4% Peak Efficiency Hybrid Converter with nH-Scale Inductors for 12 V System.....	280
<i>Tianshi Xie, Jianglin Zhu, Tom Byrd, Dragan Maksimovic, Hanh-Phuc Le</i>	
An Up to 10MHz 6.8% Minimum Duty Ratio GaN Driver with Dual-MOS-Switches Bootstrap and Adaptive Short-Pulse Based High-CMTI Level Shifter Achieving 6.05% Efficiency Improvement	282
<i>Xin Ming, Zhi-Yi Lin, Tian-Yi Sun, Yao Qin, Yuan-Yuan Liu, Chunwang Zhuang, Zhao-Ji Li, Bo Zhang</i>	
All Rivers Flow to the Sea: A High Power Density Wireless Power Receiver with Split-Dual-Path Rectification and Hybrid-Quad-Path Step-Down Conversion.....	284
<i>Zixiao Lin, Yan Lu, Fangyu Mao, Chuang Wang, Rui P. Martins</i>	

SESSION 26: QUANTUM COMPUTING AND ENERGY EFFICIENT WIRELESS TRANSCEIVERS

ULP Receivers in Self-Powered Industrial IoT Applications: Challenges and Prospects	286
<i>Kuo-Ken Huang, Jonathan K. Brown, Richard K. Sawyer, Christopher J. Lukas, Farah B. Yahya, Alice Wang, Nathan E. Roberts, Benton H. Calhoun, David D. Wentzloff</i>	
A 0.14nJ/b 200Mb/s Quasi-Balanced FSK Transceiver with Closed-Loop Modulation and Sideband Energy Detection	294
<i>Bowen Wang, Cong Ding, Yunzhao Nie, Woogeun Rhee, Zhihua Wang</i>	
A 7.25–7.75GHz 5.9mW UWB Transceiver with –23.8dBm NBI Tolerance and 1.5cm Ranging Accuracy Using Uncertain if and Pulse-Triggered Envelope/Energy Detection.....	296
<i>Bowen Wang, Haixin Song, Woogeun Rhee, Zhihua Wang</i>	
Cryogenic CMOS for Qubit Control and Readout	298
<i>Stefano Pellerano, Sushil Subramanian, Jong-Seok Park, Bishnu Patra, Todor Mladenov, Xiao Xue, Lieven M. K. Vandersypen, Masoud Babaie, Edoardo Charbon, Fabio Sebastiano</i>	

SESSION 28: HIGH-RESOLUTION AND HIGH-SECURITY DATA CONVERTERS

Design Techniques for High Linearity and Dynamic Range Digital to Analog Converters.....	306
<i>Ayman Shabra, Yun-Shiang Shu, Shon-Hang Wen, Kuan-Dar Chen</i>	
Randomized Switching SAR (RS-SAR) ADC Protections for Power and Electromagnetic Side Channel Security	314
<i>Maitreyi Ashok, Edlyn V. Levine, Anantha P. Chandrakasan</i>	

A 77 μ W 115dB-Dynamic-Range 586fA-Sensitivity Current-Domain Continuous-Time Zoom ADC with Pulse-Width-Modulated Resistor DAC and Background Offset Compensation Scheme.....	316
<i>Hao Zhang, Linxiao Shen, Shichuang Zhang, Heyi Li, Yihan Zhang, Zhichao Tan, Ru Huang, Le Ye</i>	
A 0.37mm ² 250kHz-BW 95dB-SNDR CTDSM with Low-Cost 2 nd -Order Vector-Quantizer DEM.....	318
<i>Wei Shi, Xing Wang, Xiyuan Tang, Abhishek Mukherjee, Raviteja Theertham, Shanthy Pavan, Lu Jie, Nan Sun</i>	

Author Index