# 2022 International Symposium on VLSI Technology, Systems and **Applications (VLSI-TSA 2022)**

Hsinchu, Taiwan 18 – 21 April 2022



**IEEE Catalog Number: CFP22846-POD ISBN**:

978-1-6654-0924-7

# Copyright © 2022 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP22846-POD

 ISBN (Print-On-Demand):
 978-1-6654-0924-7

 ISBN (Online):
 978-1-6654-0923-0

ISSN: 1930-8868

#### Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



## **Table of Content**

#### Session J1: Joint Plenary Session

J1-1 Latest SiC Technology and the Application Examples of Mitsubishi Electrics...1

# Session J2: Joint Special Session - Smart Edge: From Digital to Unconventional Approach (All Invited)

- J2-4 Status and Challenges of In-memory Computing for Neural Accelerators...2
- J2-5 Compute-in-memristor: A System and Technology Co-Optimization (STCO) Approach...4
- J2-6 Intelligent Vision System Using Processing-in-sensor for Smart Edge Applications...5

#### Session J3: Joint Plenary Session

J3-1 Advanced Packaging Ecosystem: Challenges and Solutions...6

# Session J5: Joint Special Session - Photonic IC Combining Circuit Design and Technologies (All invited)

- J5-1 Silicon Photonics for Next Generation Computing Systems...7
- J5-2 Development Trends of Silicon Photonics Coherent Transceivers...8
- J5-3 Hybrid Thin-film In-plane III-V/Si-related Photonic Integration...10

### Session J6: Joint Plenary Session

J6-1 Challenges and Opportunities in AI Hardware Design...11

#### **Session T1: Poster Session**

- T1-1 Performance Evaluation of 3D Memory-Logic Hybrid Bond Stacking by RLC Delay Model for Edge Computing Applications...12
- T1-2 Demonstration of 64 Conductance States and Large Dynamic Range in Sidoped HfO<sub>2</sub> FeFETs under Neuromorphic Computing Operations...14
- T1-3 Analog and Logic Circuits Fabricated on a Wafer-Scale Two-Dimensional Semiconductor...16
- T1-4 A New Cascode Design with Enhanced Power gain and Bandwidth for Application in mm-Wave Amplifier...18
- T1-5 Statistical 3D Device Simulation of Full Fluctuations of Gate-All-Around Silicon Nanosheet MOSFETs at Sub-3-nm Technology Nodes...20

- T1-6 AlInGaN/GaN HEMTs with Different GaN Cap Layer on Low Resistivity Silicon Substrate...22
- T1-7 Standby Bias Improves the Endurance in Ferroelectric Field Effect Transistors due to Fast Neutralization of Interface Traps...24
- T1-8 Tetravalent Doping in Hafnium-zirconium Oxides to Lower Polarization Switching Voltage...26
- T1-9 Novel Bit-by-bit Repair to Demonstrate STT-MRAM as NV-RAM...28
- T1-10 The Impact of Nano Device Parameters Variations and Scaling Strategy for High Frequency Performance Enhancement in Nanoscale CMOS...30
- T1-11 High-Resistivity Substrates with PN Interface Passivation in 22 nm FD-SOI...32
- T1-12 Deep Learning Approach to Modeling and Exploring Random Sources of Gate-All-Around Silicon Nanosheet MOSFETs...34
- T1-13 A Low-Power Current Readout for 77K Cryo-CMOS Quantum Systems with In-Circuit Model Extraction and Embedded Leakage-Based Temperature Monitoring...36
- T1-14 Investigation of Intrinsic Ferroelectric Switching induced Variation for Scaled FeFETs considering Limited Domain Number...38
- T1-15 Three-Zone Junction Termination Extensions for Improved Performance of Vertical GaN PN Diodes...40
- T1-16 Investigation on Selectively Etched SiGe and Si Surface for Gate-All-Around CMOS Devices Fabrication...42
- T1-17 Sensitivity Analysis of Ferroelectric Junctionless Transistors for Non-volatile Memory Applications...44
- T1-18 Effects of Channel Length on RF Performance of T-gate Poly-Si TFTs with Green Laser-Crystallized Channels...46
- T1-19 High Density Batch Bonding Technology for Chiplet Design...48
- T1-20 Study of Carrier Scattering and Mobility in Monolayer MoTe<sub>2</sub> and WTe<sub>2</sub> by First-Principle Analysis...50
- T1-21 Al<sub>2</sub>O<sub>3</sub>-HfO<sub>2</sub> Mixed High-k Dielectrics for MIM Decoupling Capacitors in the BEOL...52
- T1-22 Contacts to Two-dimensional Materials: Image Forces, Dielectric Environment, and Back-gate...54
- T1-23 The Effect of Annealing Temperature on Antiferroelectric Zirconia...56
- T1-24 Evaluation of Multi-Finger PN-Body Tied SOI-FET
  -Origin and Suppression of Stepped Id-Vg Characteristics-...58
- T1-25 Crystalline Gallium Nitride Deposition by RF-Biased Atomic Layer Annealing...60
- T1-26 A Multi-Objective Approach for Rapid Identification of Post-Cu Interconnect Candidates...62

T1-27 A Nanosized-Metal-Grain Pattern-Dependent Model for Work-Function Fluctuation of Gate-All-Around Silicon Nanofin and Nanosheet MOSFETs...64

### Session T2: Advanced Transistors for Logic and Security Applications

- T2-1 Understanding Positive Bias Stability of a-InGaZnO Thin Film Transistors with HfO<sub>2</sub> Gate Dielectric using Fast Measurement Techniques...66
- T2-2 Fin-shape Optimization for Single Diffusion Break Device Performance in FinFET Technology...68
- T2-3 6 Stacked Ge<sub>0.95</sub>Si<sub>0.05</sub> nGAAFETs without Parasitic Channels by Wet Etching...70
- T2-4 Self-Inhibit Complementary Cells by High-κ Metal Gate Transistors for Physical Unclonable Function...72
- T2-5 A Novel Physical Unclonable Function: NBTI-PUF Realized by Random Trap Fluctuation (RTF) Enhanced True Randomness in 14 nm FinFET Platform...74

#### **Session T3: Special Session-Quantum Computing (All Invited)**

- T3-1 Quantum Information Processing with Semiconductor Technology: from Qubits to Integrated Quantum Circuits...76
- T3-2 Cryo-CMOS for Quantum Computing: the road ahead...77
- T3-3 An Illustrative Sketch of a Superconducting Device...78

#### **Session T4:** Ferrorelectric

- T4-1 Analog Matrix Computing with Resistive Memory: Circuits and Theory (Invited)...79
- T4-2 Ferroelectric-Gated GaN HEMTs for RF and mm-Wave Switch Applications...81
- T4-3 Impact of Stack Structure Control and Ferroelectric Material Optimization in Novel Laminate HSO and HZO MFMIS FeFET...83
- T4-4 Characterization of Double HfZrO<sub>2</sub> based FeFET toward Low-Voltage Multi-Level Operation for High Density Nonvolatile Memory...85
- T4-5 Area Scalable Hafnium-Zirconium-Oxide Ferroelectric Capacitor Using Low-Temperature Back-End-of-Line Compatible 400°C Annealing...87

## Session T5: Advanced Memory Technology (I)

- T5-1 CeO<sub>2</sub>-Doped Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> Ferroelectrics for High Endurance Embedded Memory Applications...89
- T5-2 Cell Stability and Write Improvement of 2T (Footprint) Stacked SRAM...91
- T5-3 Development of Highly Manufacturable, Reliable, and Energy-Efficient Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM)...93

- T5-4 The Thermal Stability Improvement of Spin-orbittorque (SOT) Devices with a Thin PtMn Insertion...95
- T5-5 Proposal & Demonstration of Low Current SOT-MRAM based on Brand New Mechanism for Retention Energy of Strain-Induced Magnetic Anisotropy...97

#### **Session T6: Emerging Devices for AI**

- T6-1 The Road to Fuse With and Beyond Silicon Circuits for 2D Materials (Invited)...99
- T6-2 Anneal-Free HZO-Based Ferroelectric Field-Effect Transistor for BackEnd-of-Line-Compatible Monolithic 3D Integration...100
- T6-3 Neuromorphic Computing with Fe-FinFETs in the Presence of Variation...102
- T6-4 Pure CMOS embedded Artificial Synaptic Device (eASD) for High Density Neuromorphic Computing Chip...104
- T6-5 Improved Synaptic Characteristics in Bilayer Memristor by Post-Oxide Deposition Annealing for Pattern Recognition...106

### Session T7: Special Session-Advanced Memory Technology (II) (All Invited)

- T7-1 Spin-Transfer-Torque MRAM: The Next Revolution in Memory...108
- T7-2 New Technologies for Next-Generation MRAM...109
- T7-3 Ferroelectric Field-effect Transistors as High-density, Ultra-fast, Embedded Non-volatile Memories...110

### Session T8: Non-Fe Gate Stack & Interconnect

- T8-1 A 12nm CMOS Technology on High Performance Multi-Workfunction Transistors...111
- T8-2 Dual Gate Oxide CMOS Process on 4H-SiC...113
- T8-3 BEOL-Compatible, ALD-grown In<sub>2</sub>O<sub>3</sub> Top-Gate FETs with Maximum Drain Current of 3 A/mm through Thermal Engineering and Pulse Measurement...115
- T8-4 Lift-off-Free Complementary Carbon Nanotube FETs Fabricated With Conventional Processing in a Silicon Foundry...117
- T8-5 The Development of Accurate Model Considering the Proximity Effect to Guide the BEOL Metal Scheme Design in the Advanced Logic Device...119

# Session T9: Special Session- Low Dimensional Materials and Devices (All Invited)

- T9-1 2D Materials for Memory, Computing and 6G Applications...121
- T9-2 Latest Quantum Transport Models for Atomistic Material and Device Performance Predictions...122

- T9-3 The Manipulations of Electronic Structure and Interface Chemistry of Functionalized 2D Materials for Advanced Nanoelectronics...123
- T9-4 Surface Dynamics of Bi<sub>2</sub>Te<sub>3</sub> Measured by High Energy Resolution Photoemission Spectroscopy using a Time- and Angle-resolved Time-of-Flight Analyzer...124
- T9-5 What Are 2D Materials Good For?...125
- T9-6 Atomic-layer-deposited Atomically Thin In<sub>2</sub>O<sub>3</sub> Channel for BEOL Logic and Memory Applications...126

#### Session T10: Ferroelectric FETs and Memories

- T10-1 Integration of Multimode Sensory and Data Processing in Single-Transistor Sensors (Invited)...127
- T10-2 Improved g<sub>m</sub> and RTN Device Performance using Thick SOI in 22FDX<sup>®</sup> for Analog Applications...129
- T10-3 RF Performance Optimization of Stacked Si Nanosheet nFETs...131
- T10-4 Wide Temperature Range and High Thermal Sensitivity Radiometer Image Sensor Using CMOS SPAD Array...133
- T10-5 Si Metal-Oxide-Semiconductor and Si/SiGe Heterostructure Quantum Dots...135
- T10-6 2T-Pixel Sensors Array for on-Wafer in-Chamber DUV Sensing...137

#### Session T11: Special Session-Advanced Packaging Technologies (All Invited)

- T11-1 Advanced Packaging for HPC Platform Level Integration...139
- T11-2 Thermal Challenges in Advanced 3D System Integration: "Keeping cool while turning up the heat"...140
- T11-3 Advanced 3D Design and Technologies for 3-layer Smart Imager...141

#### **Author Index**