2021 IEEE 34th International System-on-Chip Conference (SOCC 2021)

Las Vegas, Nevada, USA
14 – 17 September 2021

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

Program for *2021 IEEE 34th International System-on-Chip Conference (SOCC)*

Time	Virtual Room I	Virtual Room 2+3
Tuesday, September 14		
05:55 am- 08:15 am		TU: *Tutorials*
Wednesday, September 15		
09:00 am- 09:15 am	*Opening Ceremony*	
09:15 am- 10:15 am	K1: *Opening Keynote Address*	
10:15 am- 10:30 am	*Break*	
10:30 am- 11:30 am	TS1: *Deep Neural Network Acceleration via FPGAs*	
11:30 am- 12:30 pm	TS2: *Future technologies and circuits and energy harvesting*	
12:30 pm- 01:30 pm	*Lunch Break*	
01:30 pm- 02:30 pm	TS3: *Novel circuits and analysis for applications*	
02:30 pm- 03:30 pm	DT: *Design Track Session*	
03:30 pm- 04:30 pm	PS1: *Poster Session I: Circuits and Systems*	
04:30 pm- 05:30 pm	SS2: *Challenges and Opportunities in AI and Big Data Applications*	

Thursday, September 16

09:00 am- 10:00 am	K2: *Keynote II: "Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems"*
10:00 am- 10:30 am	*Break*
10:30 am- 11:30 am	TS4: *Novel Workload Acceleration Techniques*
11:30 am- 12:30 pm	TS5: *Novel techniques for Security and resilience*
12:30 pm- 01:30 pm	*Lunch Break*
01:30 pm- 02:30 pm	TS6: *Advanced Power, Noise and Reliability Analysis*
02:30 pm- 03:30 pm	SS1: *Special Session 1: Hardware Security*
03:30 pm- 04:30 pm	PS2: *Poster Session II: Applications and Accelerations*
04:30 pm- 05:15 pm	SS3: *Hardware Design for Deep Neural Networks*
05:15 pm- 05:30 pm	*Closing Remarks*

Friday, September 17

06:50 am- 09:50 am	IF: *Industry Forum on High Speed SoC Interconnects (virtual only)*

Tuesday, September 14

Tuesday, September 14 5:55 - 8:15

TU: Tutorials

Virtual Room 2+3

Wednesday, September 15

Wednesday, September 15 9:00 - 9:15

Opening Ceremony

Venki Muthukumar, General Chair, Gang Qu, Technical Program Chair
Virtual Room I
Chairs: Venkatesan Muthukumar (University of Nevada Las Vegas, USA), Danella Zhao
(Old Dominion University, USA), Gang Qu (University of Maryland, USA)

Wednesday, September 15 9:15 - 10:15

K1: Opening Keynote Address

Human-Centric Computing
Prof. Jan Rabaey, CTO, STCO Division, IMEC, Belgium, and Professor, EECS Dept., Univ.
of California at Berkeley
Virtual Room I
Chair: Danella Zhao (Old Dominion University, USA)

Wednesday, September 15 10:15 - 10:30

Break

Virtual Room I

Wednesday, September 15 10:30 - 11:30

TS1: Deep Neural Network Acceleration via FPGAs

Virtual Room I

Chair: Andrew Marshall (University of Texas at Dallas, USA)

Wednesday, September 15 11:30 - 12:30

TS2: Future technologies and circuits and energy harvesting

Virtual Room I

Chair: Juergen Becker (Karlsruhe Institute of Technology, Germany)

Hugo Daniel Hernandez, Diego Augusto Pontes and Bruno Soares (Universidade Federal de Minas Gerais, Brazil); Dionísio Carvalho (University of São Paulo & USP, Brazil); Wilhelmus Van Noije (University of São Paulo, São Paulo, Brazil)

Stereolithography-Based Rectenna for Wireless Energy Harvesting...34

Xuan Viet Linh Nguyen (INSA Lyon, France); Tony Gerges (Ampere, France); Jean-Marc Duchamp (University Grenoble Alpes & G2Elab, France); Philippe Benech (Université de Grenoble-Alpes, G2ELab, France); Jacques Verdier (Institut National des Sciences Appliquées, France); Philippe Lombard (University of Lyon, France); Michel Cabrera (Université de Lyon, France); Bruno Allard (INSA Lyon, France)

Wednesday, September 15 12:30 - 1:30

Lunch Break

Virtual Room I

Wednesday, September 15 1:30 - 2:30

TS3: Novel circuits and analysis for applications

Virtual Room I

Chair: Venkatesan Muthukumar (University of Nevada Las Vegas, USA)

Software-Defined Temporal Decoupling in Virtual Platforms...40

Lukas Juenger, Alexander Belke and Rainer Leupers (RWTH Aachen University, Germany)

Embedded ICG-Based Stroke Volume Measurement System: Comparison of Discrete-Time and Continuous-Time Architectures...46

Antoine Gautier (University of Lille, Junia, France)

Analysis of the Sub-µA Fully Integrated NMOS LDO for Backscattering System...52

Puyang Zheng (Stony Brook University, USA); Xiao Sha (Stonybrook University, USA); Milutin Stanacevic (SUNY Stony Brook, USA)

A SiPM Based Sensor for Nuclear Detection Applications...57

Shahram Hatefi Hesari (The University of Tennessee, Knoxville, USA); Nicole McFarlane (University of Tennessee, USA)

Wednesday, September 15 2:30 - 3:30

DT: Design Track Session

Virtual Room I

Chair: Md Tanvir Arafin (Morgan State University, USA)

A Design Approach to Reduce Test Time on SOC Memories...63

Dieu Van Dinh (NXP Semiconductor, Inc., USA); Prokash Ghosh (NXP Semiconductor Inc & Indian Institute of Technology, Bombay, India); Misal Varma (NXP Semiconductor, Inc., India)

LC- Physical Unclonable Function in 3D Wireless IC for Securing the Internet of Things Devices...67

Jaya Dofe (California State University Fullerton, USA); Wafi Danesh (University of Missouri Kansas City, USA)

Reinforcement Learning-Based Power Management Architecture...71

David Akselrod (Advanced Micro Devices, Canada)

An Efficient Capsule Network Reconfigurable Hardware Accelerator for Deciphering Ancient Scripts with Scarce Annotations...75

Rodrigue Rizk (The Center for Advanced Computer Studies, University of Louisiana at Lafayette, USA); Dominick Rizk, Frederic Rizk and Ashok Kumar (The Center for Advanced Computer Studies University of Louisiana at Lafayette, USA); Magdy Bayoumi (University of Louisiana at Lafayette, USA)

A Cost-Efficient Reversible-Based Configurable Ring Oscillator Physical Unclonable Function...79

Dominick Rizk (The Center for Advanced Computer Studies University of Louisiana at Lafayette, USA); Rodrigue Rizk (The Center for Advanced Computer Studies, University of Louisiana at Lafayette, USA); Frederic Rizk and Ashok Kumar (The Center for Advanced Computer Studies University of Louisiana at Lafayette, USA); Magdy Bayoumi (University of Louisiana at Lafayette, USA)

Wednesday, September 15 3:30 - 4:30

PS1: Poster Session I: Circuits and Systems

Virtual Room I

Chair: Jinjun Xiong (IBM T. J. Watson Research Center, USA)

FLECSim-SoC: A Flexible End-To-End Co-Design Simulation Framework for System on Chips...83

    Tim Hotfilter, Julian Hoefer, Fabian Kreß, Fabian Kempf and Juergen Becker (Karlsruhe Institute of Technology, Germany)

Generating Hardware and Software for RISC-V Cores Generated with Rocket Chip Generator...89

    Suleyman Savas (Huawei Technologies, Switzerland); Jorn Janneck (Lund University, Sweden); Endri Bezati (EPFL SCI STI MM, Switzerland)

Implementation of an SoC Architecture with Built-In Safety Features...95

    Tibor Gergely Markovits, György Rácz and Péter Arató (Budapest University of Technology and Economics, Hungary)

Power Swapper: Approximate Functional Block Assisted Cryptosystem Security...101

    Abhijitt Dhavlle (George Mason University, USA); Setareh Rafatirad and Houman Homayoun (University of California Davis, USA); Sai Manoj Pudukotai Dinakarrao (George Mason University, USA)

TestQuBE: A Testbench Enhancement Methodology for Universal Serial Interfaces in Complex SoCs...106

    Aditya Kulkarni and Ayush Singh (Samsung Semiconductor India Research, India); Sachin Waje (National Institute of Technology Karnataka, Surathkal, India); Sunil Kashide (Samsung Semiconductor India Research, India); Seonil Choi (Samsung Electronics Co. Ltd., Korea (South))

Performance Optimization of p-Channel SnO Cylindrical Thin Film Transistors (CTFT) Using 3D Modelling...112

    Viswanath G Akkili and Viranjay M. Srivastava (University of KwaZulu-Natal, South Africa)

1.81 kHz Relaxation Oscillator with Forward Bias Comparator and Leakage Current Compensation Based Techniques...117

Xiao Sha (Stonybrook University, USA); Puyang Zheng (Stony Brook University, USA); Milutin Stanacevic (SUNY Stony Brook, USA)

Taskrunner: A Flexible Framework Optimized for Low Latency Quantum Computing Experiments...123

Richard Gebauer, Nick Karcher, Jonas Hurst and Marc Weber (Karlsruhe Institute of Technology, Germany); Oliver Sander (KIT, Germany)

Wednesday, September 15 4:30 - 5:30

SS2: Challenges and Opportunities in AI and Big Data Applications

From the Perspectives of Chip Design and Data Management

Virtual Room I

Chair: Yu-Guang Chen (National Central University, Taiwan)

Total Variation Reduction for Lossless Compression of HPC Applications...129

Huizhang Luo (Hunan University, China); Junqi Wang (Rutgers University at Newark, USA); Yida Li and Kenli Li (Hunan University, China)

Can We Trust Machine Learning for Electronic Design Automation?...135

Kang Liu (Huazhong University of Science and Technology, China); Jun Zhang (NYU, USA); Benjamin Tan (New York University, USA); Dan Feng (Huazhong University of Science and Technology, China)

Efficient Localization of Origins of PVC Based on Random Signal Segmentation...141

Dawei Li and C. Liu (South-Central University for Nationalities, China); Xiaowei Xu (Guangdong General Hospital, China)

Thursday, September 16

Thursday, September 16 9:00 - 10:00

K2: Keynote II: "Re-Engineering Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems"

Kaushik Roy, Edward G. Tiedemann Jr. Distinguished Professor, and Director C-BRIC
Purdue University, West Lafayette, IN
Virtual Room I
Chair: Jinjun Xiong (IBM T. J. Watson Research Center, USA)

Thursday, September 16 10:00 - 10:30

Break

Virtual Room I

Thursday, September 16 10:30 - 11:30

TS4: Novel Workload Acceleration Techniques

Virtual Room I
Chair: Hao Cai (Southeast University, China)
On Reduction of Computations for Threshold Function Identification...146
     Wen-Chih Hsu, Chia-Chun Lin and Yi-Ting Li (National Tsing Hua University,
     Taiwan); Yung-Chih Chen (National Taiwan University of Science and Technology,
     Taiwan); Chun-Yao Wang (National Tsing Hua University, Taiwan)
Design and Optimization of a Pruning-Efficient DCNN Inference Accelerator...152
     Che-Hao Chang and Chih-Tsun Huang (National Tsing Hua University, Taiwan)
Real-Time FPGA-Based Binocular Stereo Vision System with Semi-Global Matching
Algorithm...158
     Zhuoyu Chen, Pingcheng Dong, Zhuoao Li, Xiwei Fang, Huanshihong Deng,
     Ruoheng Yao, Yunhao Ma and Wenyue Zhang (Southern University of Science and

Technology, China); Lei Chen (Pengcheng Laboratory, China); Fengwei An
(Southern University of Science and Technology, China)

Thursday, September 16 11:30 - 12:30

TS5: Novel techniques for Security and resilience

Virtual Room I

Chair: Basel Halak (Southampton University, United Kingdom (Great Britain))

Key-Based Obfuscation Using HT-Like Trigger Circuit for 128-Bit AES Hardware IP Core...164

      Surbhi Chhabra and Kusum Lata (The LNM Institute of Information Technology,
Jaipur, India)

Identifying Specious LUTs for Satisfiability Don't Care Trojan Detection...170

      Lingjuan Wu (Huazhong Agricultural University, China); Xuefei Li, Jiacheng Zhu, Jian
Zheng and Wei Hu (Northwestern Polytechnical University, China)

ReCPE: A PE for Reconfigurable Lightweight Cryptography...176

      Jeff Anderson (The George Washington University, USA); Yousra Alkabani
(Halmstad University, Sweden); Tarek El-Ghazawi (The George Washington
University, USA)

Thursday, September 16 12:30 - 1:30

Lunch Break

Virtual Room I

Thursday, September 16 1:30 - 2:30

TS6: Advanced Power, Noise and Reliability Analysis

Virtual Room I

Chair: Lei Yang (University of New Mexico, USA)

Dynamic Power Analysis of Standard-Cell FPGA Fabrics...182

      Bo Bao and Jason Anderson (University of Toronto, Canada)

Thursday, September 16 2:30 - 3:30

SS1: Special Session 1: Hardware Security

Virtual Room I

Chairs: Md Tanvir Arafin (Morgan State University, USA), Kevin Kornegay (Morgan State University, USA)

Thursday, September 16 3:30 - 4:30

PS2: Poster Session II: Applications and Accelerations

Virtual Room I

Chair: Fakhrul Zaman Rokhani (University Putra Malaysia, Malaysia)

Nidhi Anantharajaiah (Karlsruhe Institute of Technology, Germany); Felix Knopf (Karlsruhe Institute for Technology, Germany); Juergen Becker (Karlsruhe Institute of Technology, Germany)

Design Study on Impact of Memory Access Parallelism for Cloud FPGAs...254

Arnab Ardhendu Purkayastha and Hamed Tabkhi (University of North Carolina at Charlotte, USA)

Combined Side-Channel Attacks on a Lightweight Prince Cipher Implementation...260

Soner Seckiner and Selcuk Köse (University of Rochester, USA)

GPU-Based Acceleration of Fully Parallel Annealing Algorithm for Combinatorial Optimization...N/A

Kazushi Kawamura, Kaisei Okawa, Gregory Gutmann, Thiem Chu, Jaehoon Yu and Masato Motomura (Tokyo Institute of Technology, Japan)

Thursday, September 16 4:30 - 5:15

SS3: Hardware Design for Deep Neural Networks

Virtual Room I

Chair: Yu-Guang Chen (National Central University, Taiwan)

A Convolutional Neural Network on Chip Design Methodology for CNN Hardware Implementation...266

Kun-Chih Chen, Yi-Sheng Liao and Cheng-Kang Tsai (National Sun Yat-Sen University, Taiwan)

Evaluating the Impact of Fault-Tolerance Capability of Deep Neural Networks Caused by Faults...272

Jin-Fu Li and Yung-Yu Tsai (National Central University, Taiwan)

A Hierarchical and Reconfigurable Process Element Design for Quantized Neural Networks...278

Yu-Guang Chen, Chi-Wei Hsu, Hung-Yi Chiang, Tsung-Han Hsieh and Jing-Yang Jou (National Central University, Taiwan)

Thursday, September 16 5:15 - 5:30

Closing Remarks

Virtual Room I

Friday, September 17

Friday, September 17 6:50 - 9:50

IF: Industry Forum on High Speed SoC Interconnects (virtual only)

Virtual Room I