2021 ACM/IEEE International **Workshop on System Level Interconnect Prediction** (SLIP 2021)

Virtual Workshop 4 November 2021



IEEE Catalog Number: CFP21SLP-POD ISBN:

978-1-6654-0084-8

Copyright © 2021 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP21SLP-POD

 ISBN (Print-On-Demand):
 978-1-6654-0084-8

 ISBN (Online):
 978-1-6654-0083-1

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



2021 ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP) SLIP 2021

Table of Contents

Conference Information vii Committees viii
Keynote Talk: Recent Advances and Future Challenges in 2.5D/3D Heterogeneous
Integration x Tanay Karnik (Intel, USA)
Session 1 — System Technology Co-Optimization for Advanced Physical Design
A Novel System-Level Physics-based Electromigration Modelling Framework: Application to the Power Delivery Network
Design and System Technology Co-Optimization Sensitivity Prediction for VLSI Technology Development using Machine Learning
Invited Talk: Enabling Chiplet Integration beyond 7nm
Session 2 — 3D EDA and Security
Design and Sign-off Methodologies for Wafer-to-Wafer Bonded 3D-ICs at Advanced Nodes (invited)
Invited Talk: Chip Stacking and Packaging Technology Explorations for Hardware Security 24 Makoto Nagata (Kobe University, Japan)

Performance-Aware Interconnect Delay Insertion Against EM Side-Channel Attacks	25
Session 3 — Next Generation Optical Interconnects	
Reconfigurable on-Chip Wireless Interconnections through Optical Phased Arrays (Invited) Giovanna Calo (Polytechnic University of Bari, Italy), Marina Barbiroli (University of Bologna, Italy), Gaetano Bellanca (University of Ferrara, Italy), Davide Bertozzi (University of Ferrara, Italy), Franco Fuschini (University of Bologna, Italy), Velio Tralli (University of Ferrara, Italy), Giovanni Serafino (TeCIP Institute, Scuola Superiore Sant'Anna, Italy), and Vincenzo Petruzzelli (Polytechnic University of Bari, Italy)	33
Invited Talk: Silicon Photonics Technology for Terabit-Scale Optical I/O	41
Invited Talk: Designing a Multi-chiplet Manycore System Using the POPSTAR Optical NoC Architecture	42
Train manare (elb) Listy maneey	
Session 4 — 3D Interconnects and Networks-on-Chips	
	43
Session 4 — 3D Interconnects and Networks-on-Chips Invited Talk: The Open Domain-Specific Architecture: An Introduction	
Session 4 — 3D Interconnects and Networks-on-Chips Invited Talk: The Open Domain-Specific Architecture: An Introduction	
Session 4 — 3D Interconnects and Networks-on-Chips Invited Talk: The Open Domain-Specific Architecture: An Introduction Bapi Vinnakota (Open Domain-Specific Architecture (ODSA), USA) SID-Mesh: Diagonal Mesh Topology for Silicon Interposer in 2.5D NoC with Introducing a New Routing Algorithm Babak Sharifpour (Islamic Azad University, Iran), Mohammad Sharifpour (Islamic Azad University, Iran), and Midia Reshadi (Islamic Azad	44
Session 4 — 3D Interconnects and Networks-on-Chips Invited Talk: The Open Domain-Specific Architecture: An Introduction Bapi Vinnakota (Open Domain-Specific Architecture (ODSA), USA) SID-Mesh: Diagonal Mesh Topology for Silicon Interposer in 2.5D NoC with Introducing a New Routing Algorithm Babak Sharifpour (Islamic Azad University, Iran), Mohammad Sharifpour (Islamic Azad University, Iran), and Midia Reshadi (Islamic Azad University, Iran) RAMAN: Reinforcement Learning Inspired Algorithm for Mapping Applications onto Mesh Network-on-Chip Jitesh Choudhary (BITS-Pilani, Hyderabad Campus, India), Soumya J (BITS-Pilani, Hyderabad Campus, India), and Linga Reddy Cenkeramaddi	44