

2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC 2021)

**Virtual Conference
1 – 3 December 2021**



**IEEE Catalog Number: CFP21453-POD
ISBN: 978-1-6654-1620-7**

**Copyright © 2021 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP21453-POD
ISBN (Print-On-Demand):	978-1-6654-1620-7
ISBN (Online):	978-1-6654-1619-1

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Table of Contents (Conference)

Content Type	Description
Title Page	Page I
Table of Contents	Page II
Paper Title List	Page III - XI

Paper Title list.

paper ID	Page no.	Full Manuscript	Copyright Identifier	Paper Title
100	530 - 537	100P2021168983.pdf	100	Roadmap Based on Holistic Understanding of Thermo-Mechanical Challenges from Package to System to Maximize Silicon Performance
101	538 - 546	101P2021159082.pdf	101	Nonlinear Thermal Stress/Strain Analyses of Through SiC Via
102	45 - 49	102P2021161409.pdf	102	Localization of Hotspots from Lock-in Thermography Images for Failure Analysis
103	50 - 52	103P2021152947.pdf	103	Failure Analysis & Mechanism Studies of the Worm-like Defects in Vias of Wafer Fabrication
104	53 - 55	104P2021152950.pdf	104	Failure Analysis and Elimination of the Bromine-induced Defects in Wafer Fabrication
105	473 - 478	105P2021243104.pdf	105	Current Crowding Effects on the Thermal Performance of AlGaIn/GaN Light Emitting Diodes
106	184 - 189	106P2021197489.pdf	106	Investigation of Thermoelectric Cooling for a Competition Electric Vehicle
107	56 - 59	107PID.pdf	107	Electrochemical Migration Failure under Biased HAST due to Photoresist Residues
110	677 - 681	110P2021168423.pdf	110	Polarization-Insensitive Metalenses at Wavelengths in Ultraviolet Region
111	547 - 552	111P2021198760.pdf	111	Package Warpage Modeling by Considering Shrinkage Behavior of EMC and Substrate
112	479 - 482	112P2021194057.pdf	112	Thermal characterization of automotive power module with SHERPA
113	483 - 487	113P2021193717.pdf	113	Non-contact thermal characterization using IR camera for compact metal-oxide gas sensor
114	121 - 125	114P2021215515.pdf	114	Intermetallic growth and void formation mechanism in flip chip copper pillar interconnects: role of the underfill material
116	60 - 65	116P2021201406.pdf	116	Foreign Materials Management: A Critical but Overlooked Element in Optoelectronic Device Introduction
117	413 - 418	117P2021205550.pdf	117	Influence of BGA Design Parameters on Solder Joint Reliability

118	190 - 194	118P2021187787.pdf	118	Molecular dynamics study of BNNS/Al composites under compression
119	620 - 623	119P2021200172.pdf	119	High Reliability Solution of 2.5D Package Technologies
120	265 - 269	120P2021200752.pdf	120	Development of an Innovative Leadframe Design for Eliminating Lead Delamination
121	126 - 130	121P2021201724.pdf	121	Advanced Thermal Lid Attach Adhesive for High Performance Computing (HPC) Package
122	419 - 422	122P2021215298.pdf	122	Effects of Sb and Bi addition on IMC morphology and reliability of Pb-free solder/Cu-OSP
123	553 - 562	1232021199000.pdf	123	Simulation of Moisture Ingression in Microelectronics Package to Correlate Tests and Field Conditions
124	1 - 7	124P2021202124.pdf	124	Cu-Cu Thermocompression Bonding with Cu-Nanowire Films for Power Semiconductor Die-Attach on DBC Substrates
125	108 - 110	125P2021201694.pdf	125	Printing an anisotropic conductive film for structural electronics applications
126	423 - 426	126P2021208203.pdf	126	Low Temperature Solder Paste Characterization during Memory Module and SSD Product Level Reliability Test
127	427 - 429	127P2021198067.pdf	127	Comparative Study of Solder Strength Characterization for BGA Packages
128	91 - 92	128P2021198930.pdf	128	2D X-Ray Void Detection for Next Generation Copper Pillar Bump
129	93 - 94	129P2021198976.pdf	129	X-ray inspection for FOMCM (Fan-Out Multi Chip Module)
130	201 - 204	130P2021213584.pdf	130	Parametric Study of Gravure Printing for Electric Heaters
131	131 - 133	131P2021201246.pdf	131	Dispensing Process of Silver Adhesive to Minimize the Joint Surface Area-to-Volume Ratio for Premature Dried Adhesives Prevention
133	322 - 325	133P2021198063.pdf	133	High Efficient RF Energy Harvesting Circuit using Cascade Structure
134	326 - 329	134P2021187733.pdf	134	Terahertz band on-chip one-sided directional wide band slot array antenna
135	330 - 333	135P2021187657.pdf	135	One-sided directional slot array antenna for 28GHz wideband operation

137	334 - 338	137P2021186022.pdf	137	Alternative Low Cost EMI Shielding Solutions of SiP Module for 5G mmWave Applications
138	288 - 291	138P2021198481.pdf	138	Investigations on Silver Sintering using an Ultrasonic Transient Liquid Phase Sintering Process
139	563 - 567	139P2021200427.pdf	139	Study of Laser Ablation Slits in Stress Reduced Embedded Die Substrate Fabricated for Heterogeneous Integration
140	624 - 627	140P2021205936.pdf	140	Low Temperature Physical Vapour Deposited Cu Seed Layer for Temporary Bonded Wafer Substrates
141	568 - 572	141P2021215338.pdf	141	A comparative study of stress-based and fracture mechanics-based finite element simulation approaches for RDL based wafer level package
142	573 - 578	142P2021201635.pdf	142	Numerical study on wafer level warpage evolution during chip to wafer hybrid bonding process
143	488 - 492	143P2021200612.pdf	143	Thermal characterization of battery cold plates
144	628 - 632	144P2021201278.pdf	144	Heating Dissipation Discussion of TSV-integrated Ion Trap with Glass Interposer
145	134 - 139	145P2021215392.pdf	145	Fine Pitch Microdots Dispensing and Jetting Optimization in SiP Assembly using Welco Solder Paste
146	493 - 496	146P2021200319.pdf	146	Embedded Cooling for High Heat Flux Hot Spots in Different Sizes
147	213 - 217	147P.pdf	147	Diffusion and oxidation of copper in polymer of Fan Out-Panel Level Package (FO-PLP) under High Temperature Storage (HTS) Conditions
148	363 - 368	148P2021198908.pdf	148	An Effective Coding Transmission Scheme for TSV Array Transmission with Defects
149	218 - 221	149P2021193107.pdf	149	Investigation on the reliability risk for high density Fan-Out packages
150	430 - 434	150P2021202250.pdf	150	Comprehensive Study on Thermal Aging and Ball Shear Characterization of SAC-X Solders
151	222 - 225	151P2021198185.pdf	151	Fan-Out Embedded Bridge Solution in HPC Application
152	633 - 636	152P2021191151.pdf	152	Development of Metallization Process for Fine Pitch TSV
153	140 - 143	153P2021200371.pdf	153	Systematic Investigation and Characterization of Ag Paste for LED Die Attach

154	435 - 439	154P2021195471.pdf	154	Application of EBSD Study of Cu-Sn IMCs in SAC305 and Sn0.7Cu Solder Joints to Determine the Suitability of Sn0.7Cu Solder as Alternative in Mitigating ILD Cracks/Delamination
155	226 - 230	155P2021213191.pdf	155	Fabrication Process Flow of Antenna-in-Package Fan-out Wafer Level Packaging
156	8 - 12	156P2021202935.pdf	156	Atomistic-scale Simulations on Surface Activation Process of Dielectric Oxides for Hybrid Bonding Applications
157	369 - 373	157P2021208936.pdf	157	Systematic Signal Integrity Analysis on Fine Pitch Probe Card for HBM Interposer Testing
158	374 - 377	158P2021202099.pdf	158	Die Attach Effect on Electrical Performance and Reliability of Embedded Die Package
159	659 - 663	159P2021200112.pdf	159	Development of UV Curable Wafer Back Side Protection-Film for Wafer Level Chip Size Package
160	440 - 444	160P2021200625.pdf	160	Copper wire degradation under high temperature and high humidity without molding compound
161	579 - 582	161P2021203007.pdf	161	Mechanical Robustness study of Ultra Low profile 3D Silicon capacitors
162	445 - 450	162P2021200350.pdf	162	Effect of Pneumatic Reflow Profiling on Voiding Reduction in High-Lead Solder Die Attach
163	270 - 275	163P2021220198.pdf	163	Flexible Integrated Battery on System-in-Package (SiP) for Internet of Things (IoT) and Smart Wearables
164	378 - 380	164P2021198992.pdf	164	Design and Implementation of a Ka-Ku Frequency Conversion Receiver 3D SiP Module
165	451 - 459	165P2021200953.pdf	165	Interfacial reaction and mechanical properties of Cu/Ga/Cu interconnects during the transient liquid phase bonding
166	195 - 200	166P2021199614.pdf	166	MAXQFP: NXP new package platform
167	664 - 667	167P2021210976.pdf	167	Silicon Isolation Trench Integration for the 4-stack Memory Wafer
168	235 - 238	168P2021199704.pdf	168	Dual Polarized FOWLPAiP for 5G Base Station Applications
169	339 - 342	169P2021199855.pdf	169	Development of a wide-band compact diplexer using a redistribution layer for 5G application
171	292 - 296	171P2021225405.pdf	171	Effect of Nickel, Silver, and Gold Wafer Backside Metallization (BSM) on 80Au20Sn (Gold-Tin) Die Attach

172	148 - 152	172P2021200187.pdf	172	Investigation of the flow behaviors for capillary underfill process in flip chip packaging
174	276 - 278	174P2021209463.pdf	174	Surface Plasma and Mold Deflash Treatment of Plated and Non-Plated Cu Leadframe for Leadframe-to-Mold Adhesion Improvement
176	297 - 301	176P2021229374.pdf	176	Study on the Impacts of Clamping Process Defects to the Reliability of Press-Pack IGBTs
178	239 - 243	178P2021194137.pdf	178	Large Size Multilayered Fan-Out RDL Packaging for Heterogeneous Integration
179	153 - 156	179P2021201648.pdf	179	Die Attach Material Optimization for Enhancing Package Integrity of Surface Mount Device after Moisture Sensitivity Level 1
180	497 - 502	180P2021200773.pdf	180	Analysis of Evaporation from micropillar surface by Using Non-Uniform Heat Flux
181	66 - 73	181P2021202480.pdf	181	Understanding Sulfur-Induced Surface Discoloration of QFN-mr Leads After Prolonged Environmental Exposure
182	387 - 391	182P2021203279.pdf	182	Signal integrity analysis of butterfly-shaped vias for RF packages
183	13 - 17	183P2021198866.pdf	183	Realization of High Aspect Ratio Through Mold Interconnect (TMI) using Vertical Wire
188	343 - 346	188P2021202456.pdf	188	RF Performance Study of Through-Mold-Via (TMV) using L-2L De-Embedding Method
190	279 - 283	190P2021202241.pdf	190	Determination of Optimal Setting for the Tape-Based Partial Package Sawing of Wettable Flank QFN Package
191	392 - 394	191P2021220715.pdf	191	A generic approach for automatic design rule derivation for assembly design kits (ADK)
192	395 - 398	192P2021218198.pdf	192	Bunch of Wires Interface PHY Design for Multi-Chiplet Systems
193	157 - 162	193P2021214055.pdf	193	Microelectronic Encapsulant Material Assessment: A Security Point of View
194	23 - 27	194P2021225417.pdf	194	Characteristics of Plasma Treated Surface for SiO ₂ -Si Wafer Bonding
195	399 - 404	195P2021217589.pdf	195	On the Correction of the Effects of Electrical transients in the Measured Thermal Transients
198	244 - 247	198P2021209302.pdf	198	Shear Performance and Accelerated Reliability of 6 x 6 mm ² FOWLP Solder Joints using an ENIG based PCB Electrode

199	347 - 350	199P2021205632.pdf	199	Assembly and Packaging of Miniature Nanoantenna Spatial Light Modulator
200	405 - 409	200P2021214952.pdf	200	Testing Multiple High Speed Channels using Automated Test Equipment(ATE), SOC 93K, in parallel
201	668 - 671	201P2021219413.pdf	201	Thin Wafer De-bonding for 3D-TSV Packaging of High Bandwidth Memory Devices using UV Irradiation
202	460 - 463	202P2021214052.pdf	202	Effects of Co on the Morphology, Shear Strength and Fracture of the Low temperature SAC305/Sn-58Bi/Cu Composite Solder Joint
203	351 - 356	203P2021216321.pdf	203	Addressing the assembly challenges of Antenna-in-package
204	248 - 252	204P2021227154.pdf	204	Heterogeneous Integration on Fan-Out Wafer Level Packaging Plat Form
205	503 - 507	205P2021200688.pdf	205	Thermal effect investigation of chip-to-wafer hybrid bonding on 3D-stacked memory
206	672 - 676	206P2021208421.pdf	206	SAW Cavity Sealing using Dielectric film in Wafer-level packaging
207	637 - 641	207P2021251402.pdf	207	Low Temperature Oxide Passivation for Via-last/backside process
208	642 - 648	208P2021214511.pdf	208	High Density Redistribution Layers (< 2 um L/S) for Chiplets Packaging
209	302 - 308	209P2021169719.pdf	209	Progress on low temperature sintering of nano-silver
210	253 - 257	210P2021212951.pdf	210	Through Mold Via Development Using Laser Drilling Process for 3D Fan-out Wafer Level Package
211	18 - 22	211P2021213007.pdf	211	Comprehensive Study on Polymer Based Chip-to/chip Bonding For Gas Sensor Application
212	28 - 32	212P2021215710.pdf	212	Cu CMP Dishing in High Density Cu Pad for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding
213	284 - 287	213P2021199941.pdf	213	Pressure Sensor Substrate for Prolonged Sitting and Posture Monitoring
214	508 - 512	214P2021206656.pdf	214	Thermal design and analysis for double side cooling 6-in-1 SiC power module
215	74 - 79	215P2021199780.pdf	215	Failure Mechanism and Prevention of Die Cracking for FBGA Package Mislaced in the Tray
216	205 - 208	216P2021200025.pdf	216	Reference Free Ion-Selective Electrode for sensing Potassium Ions

217	589 - 593	217P2021215514.pdf	217	Mechanical modeling study for fan-out wafer level package parameters to enhance BGA TCoB life
218	513 - 518	218P2021202949.pdf	218	Numerical investigation of the optimization on manifold microchannel heat sink towards the water-cooling limit
219	95 - 98	219P2021199952.pdf	219	Thick films of polymer Direct-conversion X-ray detectors
220	99 - 103	220P2021193258.pdf	220	Organic Panel Fine Circuit Pattern Inspection and Metrology for Readiness
221	649 - 652	221P2021214205.pdf	221	A 2.5D Heterogeneous Integration Demonstration for High Performance RF Application using High-Resistivity Through Si Interposer (TSI)
222	594 - 599	222P2021198297.pdf	222	Thermo-Mechanical load Influence on Electronics Packages
223	33 - 36	223P2021215453.pdf	223	Wafer-to-Wafer Hybrid Bonding Challenges for 3D IC Applications
224	600 - 604	224P2021216004.pdf	224	The Effect of Adhesive and Carrier Material Properties on Thermo-Mechanical Stresses of GaSb, InSb Semiconductors due to Cryocooling
225	357 - 362	225P2021201714.pdf	225	High density packaging techniques for miniaturization of satellite RF and microwave subsystems: Attachments, Interconnections and Hermetic sealing
227	605 - 608	227P2021202441.pdf	227	Design Selection and Optimization of Mechanical Anchoring Structure on Pre-plated Cu Leadframes
228	381 - 386	228P2021198320.pdf	228	Evaluation of Contact Conductance and Its Importance in Electronic Packaging
229	609 - 615	229P2021199037.pdf	229	Fatigue behaviour of small-sized in-situ packaging materials based on a single-point nanoindentation with cycle penetrations
230	464 - 468	230P2021198830.pdf	230	Growth kinetics of intermetallic compound in solder joints during thermal cycling: a review.
231	410 - 412	231P2021187713.pdf	231	Chiplet-based Architecture Design for Multi-Core Neuromorphic Processor
232	519 - 523	232P2021217530.pdf	232	Heat Sink Employing Straight Microchannels with Sidewall Ribs in Staggered Arrangement for Liquid Based Cooling of Microelectronic Chips
233	163 - 169	233P2021202041.pdf	233	Effect of Moisture in a Non-conductive Glue on the Electrical Performance of a Cavity Package

234	309 - 316	234P2021199116.pdf	234	Influence of Packaging Structure on Switch Performance of GaN HEMT Half-Bridge Circuits
235	37 - 41	235P2021214909.pdf	235	Towards Heterogeneous Integrated Electronic-Photonic Packages for Hyperscale Data Centers
236	170 - 175	236P2021202974.pdf	236	Acceleration Factor For Polymer Degradation by UV Light Exposure
238	469 - 472	238P2021222402.pdf	238	Study on Mechanical Behavior and Long-term Storage Reliability of Micron-level Mixed Solder Joints
239	317 - 321	239P2021199640.pdf	239	Porosity effect on fracture behaviour of sintered silver nanoparticles by phase-field modelling
240	258 - 264	240P2021192320.pdf	240	Deca & ASE Scaling M-Series & Adaptive Patterning to 600mm
241	209 - 212	241P2021215423.pdf	241	Degradation of SOI SRAMs at 250°C operating conditions
242	104 - 107	242P2021199191.pdf	242	Detecting Wire Bond Inter Layer Dielectric Crack by Dark Field Imaging
243	42 - 44	243P2021218283.pdf	243	Successful heterogeneous integration of chiplet's demands "shift-left" system level optimization
244	653 - 658	244P2021203366.pdf	244	Effect of Via Placement on Wafer-Level Packaged Resonant MEMS Structures
245	616 - 619	245P2021202436.pdf	245	Determining mechanical properties of thin film in packaging structures by in-situ nanoindentation
246	524 - 529	246PID.pdf	246	Numerical Model for Understanding Interconnection Thermal Reliability Mechanism of Cu Via in Back End of Line (BEOL)
248	231 - 234	248P2021201576.pdf	248	Hybrid RDL Design in Fan-out Package
250	111 - 114	250P2021205095.pdf	250	Flow and Gauge Sensor Fusion in Vapour Phase Soldering Ovens for Optimized Process Control
251	176 - 183	251P2021217405.pdf	251	Development of Build-up Dielectric Material that enables High Temp. Low Loss, High Fracture Toughness Advanced FC-BGA Substrates
254	80 - 84	254P2021203342.pdf	254	Developments in Advanced Packaging Failure Analysis using Correlated X-Ray Microscopy and LaserFIB
255	85 - 90	255P2021218324.pdf	255	Non-destructive thermal diagnostics of multilayer substrates for multichip modules

256	144 - 147	256P2021201656.pdf	256	Dicing Blade Characterization Using Nano-indentation
257	115 - 120	257P2446.pdf	257	Kulicke & Soffa: Enabling predictive analytic through deep learning