

2021 International Conference on Field-Programmable Technology (ICFPT 2021)

**Virtual Conference
6-10 December 2021**



IEEE Catalog Number: CFP21528-POD
ISBN: 978-1-6654-2011-2

**Copyright © 2021 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP21528-POD
ISBN (Print-On-Demand):	978-1-6654-2011-2
ISBN (Online):	978-1-6654-2010-5

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Table of Contents

Machine Learning

LETA: A Lightweight Exchangeable-Track Accelerator for EfficientNet Based on FPGA	1
<i>Jingbo Gao, Yu Qian, Yihan Hu, Xitian Fan, Wai-Shing Luk, Wei Cao and Lingli Wang</i>	
Efficient Stride 2 Winograd Convolution Method Using Unified Transformation Matrices on FPGA	10
<i>Chengcheng Huang, Xiaoxiao Dong, Zhao Li, Tengting Song, Zhenguo Liu and Lele Dong</i>	
Optimizing Bayesian Recurrent Neural Networks on an FPGA-based Accelerator	19
<i>Martin Ferianc, Zhiqiang Que, Hongxiang Fan, Wayne Luk and Miguel Rodrigues</i>	
A High-Performance and Flexible FPGA Inference Accelerator for Decision Forests Based on Prior Feature Space Partitioning	29
<i>Thiem Van Chu, Ryuichi Kitajima, Kazushi Kawamura, Jaehoon Yu and Masato Motomura</i>	

Machine Learning (Short Papers)

Low Precision Networks for Efficient Inference on FPGAs	39
<i>Ruth Abra, Dmitry Denisenko, Richard Allen, Tim Vanderhoek, Sarah Wolstencroft and Mark Gibson</i>	

High Level Synthesis and Electronic Design Automation

FLOWER: A Comprehensive Dataflow Compiler for High-Level Synthesis	44
<i>Puya Amiri, Arsène Pérard-Gayot, Richard Membarth, Philipp Slusallek, Roland Leißa and Sebastian Hack</i>	

High Level Synthesis and Electronic Design Automation (Short Papers)

AMAH-Flex: A Modular and Highly Flexible Tool for Generating Relocatable Systems on FPGAs	53
<i>Najdet Charaf, Christoph Tietz, Michael Raitza, Akash Kumar and Diana Goehringer</i>	
Profiling-Based Control-Flow Reduction in High-Level Synthesis	59
<i>Austin Liolli, Omar Ragheb and Jason Anderson</i>	
On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators	65
<i>Tiago Santos, Nuno Paulino, João Bispo, João M. P. Cardoso and João C. Ferreira</i>	

Mathematical Computations and Digital Signal Processing

StreamSVD: Low-rank Approximation and Streaming Accelerator Co-design	69
<i>Zhewen Yu and Christos-Savvas Bouganis</i>	

High Performance Lattice Regression on FPGAs via a High Level Hardware Description Language	78
<i>Nathan Zhang, Matthew Feldman and Kunle Olukotun</i>	

Mathematical Computations and Digital Signal Processing (Short Papers)

Dataflow Systolic Array Implementations of Exploring Dual-Triangular Structure in QR Decomposition Using High Level Synthesis	88
<i>Siyang Jiang, Hsi-Wen Chen and Ming-Syan Chen</i>	
Exponential Sine Sweep Measurement Implementation Targeting FPGA Platforms	92
<i>Alexander Klemd, Patrick Nowak, Piero Rivera Benois, Etienne Gerat, Bernd Klauer and Udo Zölzer</i>	
Parallel-Pipeline Fast Walsh-Hadamard Transform Implementation Using HLS	98
<i>Andres Manjarrés García, Carlos Osorio Quero, Jose Rangel-Magdaleno, Jose Martinez-Carranza and Daniel Durini</i>	
FPGAs as General-Purpose Accelerators for Non-Experts via HLS: The Graph Analysis Example	102
<i>Pedro Filipe Silva, João Bispo and Nuno Paulino</i>	

Image Processing and Computer Vision

ac ² SLAM: FPGA Accelerated High-Accuracy SLAM with Heapsort and Parallel Keypoint Extractor	106
<i>Cheng Wang, Yingkun Liu, Kedai Zuo, Jianming Tong, Yan Ding and Pengju Ren</i>	
A Streaming Hardware Architecture for Real-Time SIFT Feature Extraction	115
<i>Hector Li Sanchez and Alan George</i>	
A Unified Accelerator Design for LiDAR SLAM Algorithms for Low-end FPGAs	124
<i>Keisuke Sugiura and Hiroki Matsutani</i>	
Algorithm-Hardware Co-Optimization for Energy-Efficient Drone Detection on Resource-Constrained FPGA	133
<i>Han-sok Suh, Jian Meng, Ty Nguyen, Shreyas Kolala Venkataramanaiah, Vijay Kumar, Yu Cao and Jae-sun Seo</i>	

Image Processing and Computer Vision (Short Papers)

Energy-efficient FPGA-accelerated LiDAR-based SLAM for Embedded Robotics	142
<i>Mario Porrman, Thomas Wiemann, Marc Rothmann, Marco Tassemeier, Marc Eisoldt, Julian Gaal and Marcel Flottmann</i>	

Architecture and Devices

General Routing Architecture Modelling and Exploration for Modern FPGAs	148
<i>Jiadong Qian, Yuhang Shen, Kaichuang Shi, Hao Zhou and Lingli Wang</i>	
FastCGRA: A Modeling, Evaluation, and Exploration Platform for Large-Scale Coarse-Grained Reconfigurable Arrays	157
<i>Su Zheng, Kaisen Zhang, Yaoguang Tian, Wenbo Yin, Lingli Wang and Xuegong Zhou</i>	

APIR-DSP: An Approximate PIR-DSP Architecture for Error-Tolerant Applications	167
<i>Yuan Dai, Simin Liu, Yao Lu, Hao Zhou, Seyedramin Rasoulinezhad, Philip H.W. Leong and Lingli Wang</i>	

Architecture and Devices (Short Papers)

Characterization of IOBUF-based Ring Oscillators	175
<i>Julia Burgiel, Daniel Esguerra, Ilias Giechaskiel, Shanquan Tian and Jakub Szefer</i>	
A Hexagon-Based Honeycomb Routing Architecture for FPGA	179
<i>Kaichuang Shi, Hao Zhou and Lingli Wang</i>	

Networks and Data Management

Increasing Memory Efficiency of Hash-Based Pattern Matching for High-Speed Networks .	185
<i>Tomáš Fukáč, Jiří Matoušek, Jan Kořenek and Lukáš Kekely</i>	
Tens of gigabytes per second JSON-to-Arrow conversion with FPGA accelerators	194
<i>Johan Peltenburg, Ákos Hadnagy, Matthijs Brobbel, Robert Morrow and Zaid Al-Ars</i>	
StreamZip: Compressed Sliding-Windows for Stream Aggregation	203
<i>Prajith Ramakrishnan Geethakumari and Ioannis Sourdis</i>	
Scalable and Flexible High-Performance In-Network Processing of Hash Joins in Distributed Databases	212
<i>Johannes Wirth, Jaco Hofmann, Lasse Thostrup, Carsten Binnig and Andreas Koch</i>	

Networks and Data Management (Short Papers)

Efficient Queue-Balancing Switch for FPGAs	221
<i>Philippos Papaphilippou, Kentaro Sano, Boma A. Adhi and Wayne Luk</i>	

Systems and Security

Efficient Physical Page Migrations in Shared Virtual Memory Reconfigurable Computing Systems	226
<i>Torben Kalkhof and Andreas Koch</i>	
StateLink: FPGA System Debugging via Flexible Simulation/Hardware Integration	236
<i>Sameh Attia and Vaughn Betz</i>	

Systems and Security (Short Papers)

In-Storage Computation of Histograms with Differential Privacy	246
<i>Andrei Tosa, Anca Hangan, Gheorghe Sebestyen and Zsolt István</i>	

Physical Computations

High-Performance Hardware Implementation of CRYSTALS-Dilithium	250
<i>Luke Beckwith, Duc Nguyen and Kris Gaj</i>	
A Modular RFSoc-based Approach to Interface Superconducting Quantum Bits	260
<i>Richard Gebauer, Nick Karcher and Oliver Sander</i>	

An Efficient RTL Buffering Scheme for an FPGA-Accelerated Simulation of Diffuse Radiative Transfer	269
<i>Kazuki Furukawa, Tomoya Yokono, Yoshiki Yamaguchi, Kohji Yoshikawa, Norihisa Fujita, Ryohei Kobayashi, Taisuke Boku and Masayuki Umemura</i>	

Physical Computations (Short Papers)

Total-ionizing-dose tolerance evaluation of an optoelectronic field programmable gate array VLSI in operation	278
<i>Hiroshi Ito and Minoru Watanabe</i>	

PhD Forum papers

A High-Precision Flexible Symmetry-Aware Architecture for Element-Wise Activation Functions	282
<i>Xuan Feng, Yue Li, Yu Qian, Jingbo Gao, Wei Cao and Lingli Wang</i>	
High-performance pipeline architecture for packet classification accelerator in DPU	286
<i>Jing Tan, Gaofeng Lv, Yanni Ma and Guanjie Qiao</i>	
Parallelized Technology Mapping to General PLBs by Adaptive Circuit Partitioning	290
<i>Xiaoxi Wang, Moucheng Yang, Zhen Li and Lingli Wang</i>	
Resource-saving FPGA Implementation of the Satisfiability Problem Solver: AmoebaSATslim	295
<i>Yingjie Yan, Hideharu Amano, Masashi Aono, Kaori Okoda, Shingo Fukuda, Kenta Saito and Seiya Kasai</i>	
An area-efficient multiply-accumulation architecture and implementations for time-domain neural processing	300
<i>Ichiro Kawashima, Yuichi Katori, Takashi Morie and Hakaru Tamukoh</i>	
Real-time Implementation of Cyclostationary Analysis using FPGAs	304
<i>Jingyi Li</i>	

Design Competition papers

An Autonomous Driving System Utilizing Image Processing Accelerated by FPGA	308
<i>Kazunari Takasaki, Kota Hisafuru, Ryotaro Negishi, Kazuki Yamashita, Keisuke Fukada, Tomoya Wakaizumi and Nozomu Togawa</i>	
An FPGA-based Image Recognition with Remote Update Functions for Autonomous Driving on "ad-refkit"	312
<i>Hyuga Hashimoto, Ryo Naka and Yasutaka Wada</i>	
SoC FPGA Implementation of an Unmanned Mobile Vehicle with an Image Transmission System over VNC	315
<i>Keigo Motoyoshi, Yuta Imamura, Taichi Saikai, Koki Fujita, Daiki Furukawa, Masatomo Matsuda, Tatsuma Mori, Yasutoshi Araki, Takehiro Miura, Keizo Yamashita, Haruto Ikehara, Kaito Ohira, Katsuaki Kamimae, Takaho Kawazu, Masahiro Nishimura, Shintaro Matsui, Koki Tomonaga, Taito Manabe and Yuichiro Shibata</i>	

Zytlebot : FPGA Integrated ROS-Based Autonomous Mobile Robot.....	319
<i>Ryota Miyagi, Sho Kinoshita, Masashi Oda, Naofumi Takagi and Hideki Takase</i>	
Autonomous Driving System implemented on Robot Car using SoC FPGA	323
<i>Akira Kojima</i>	
Development of Autonomous Driving System based on Image Recognition using Programmable SoCs	327
<i>Ryohei Yamamoto, Yuki Izumi, Ryo Aono, Takumi Nagahara, Tomonari Tanaka, Wang Laio and Yukio Mitsuyama</i>	
A Dataset Generation for Object Recognition and a Tool for Generating ROS2 FPGA Node.....	331
<i>Hayato Amano, Hayato Mori, Akinobu Mizutani, Tomohiro Ono, Yuma Yoshimoto, Takeshi Ohkawa and Hakaru Tamukoh</i>	
Fast Controlling Autonomous Vehicle Based on Real Time Image Processing	335
<i>Hamed Jani, Mohammad Mahdi Gohari, Amir Hossein Heydariyan, Mostafa Lashkari, Mohamad Reza Lashkari and Hossein Borhanifar</i>	