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Program

Monday, September 27

Breakfast 7:30 − 8:30

Session: Plenary I (Monet)

P01 8:30 – 9:30 ***Plenary Talk***: **TCAD for logic technology process development**.....**1**
Stephen M. Cea, S. Berrada, K. Ghosh, S. Hasan, P. Keys, R. Mehandru, B. Obradovic, V. Tiwari, C. Weber, and M. Stettler (Logic Technology Division, Intel Corporation, Hillsboro, OR, USA)

Break 9:30 − 9:50

Session 1: Advanced Scaling and SRAM (Monet)

Chairperson
Oskar Baumgartner (Global TCAD Solutions, Austria)

S1.1 9:50 – 10:20 ***Invited Talk***: **TCAD challenges and opportunities to find a feasible device architecture for sub-3nm scaling.**.....**5**
Uihui Kwon, Yonghee Park, Yoon-Suk Kim, Jaehyun Yoo, and Dae Sin Kim (CSE Team, DIT Center, Samsung Electronics Corp. Ltd., Korea)

S1.2 10:20 – 10:40 **Complementary FET for Advanced Technology Nodes: Where Does It Stand?.**.....**11**
Liu Jiang, Ashish Pal, El Mehdi Bazizi, He Ren, Mehul Naik, Blessy Alexander, and Buvna Ayyagari (Applied Materials Inc., Santa Clara, California, USA)

S1.3 10:40 – 11:00 **Variability-Aware DTCO Flow: Projections to N3 FinFET and Nanosheet 6T SRAM.**.....**15**
M. Karner, G. Rzepa, O. Baumgartner, G. Strof, F. Schanovsky, F. Mitterbauer, C. Kernstock, H. W. Karner, and Z. Stanojevic (Global TCAD Solutions, Vienna, Austria)

S1.4 11:00 – 11:20 **Nanosheet Width Investigation for Gate-All-Around Devices Targeting SRAM Application.**.....**19**
Ashish Pal, El Mehdi Bazizi, Benjamin Colombeau, Blessy Alexander, and Buvna Ayyagari-Sangamalli (Applied Materials, Santa Clara, USA)

S1.5 11:20 – 11:40 **Combined Process Simulation and Emulation of an SRAM Cell of the 5nm Technology Node**.....**23**
Xaver Klemenschits, Siegfried Selberherr, and Lado Filipovic (Institute

Break 4:00 – 4:15

4:15 – 6:00 **On-site paper discussion** (Monet)

6:00 – 7:00 **Reception** (Break area)

Tuesday, September 28

Wednesday, September 29

Thursday, September 30

7:30 − 8:30 **Virtual paper discussion**