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Virtual Conference 6 – 8 October 2021



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34th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems Technical Program

(DFT **2021**)

October 6-8, 2021

The time is in CEST zone

- (L) stands for Long papers and (S) starts for Short papers
- The duration of the prerecorded presentations is 15 to 20 minutes. The duration of the live presentation of each paper is 15 minutes (5 to 7 minutes live talk and Q&A)

DAY 1 - Wednesday October 6, 2021

14:45 - 15:10: Starting Session

General Chairs' Welcome Message Program Overview Instructions by A/V chair

15:10 - 16:10: Session #1 - Neural networks

- (L) Analyzing the Single Event Upset Vulnerability of Binarized Neural Networks on SRAM FPGAs...1 Ioanna Souvatzoglou, Athanasios Papadimitriou, Aitzan Sari, Vasileios Vlagkoulis and Mihalis Psarakis
- (L) Zero-Overhead Protection for CNN Weights...7 Stéphane Burel, Adrian Evans and Lorena Anghel
- (L) Fine-Grained Vulnerability Analysis of Resource Constrained Neural Inference Accelerators...13 Panayiotis Corneliou, Panagiota Nikolaou, Maria K. Michael and Theocharis Theocharides
- (S) The Impact of Faults on DNNs: A Case Study...19 Elaheh Malekzadeh, Nezam Rohbani, Zhonghai Lu and Masoumeh Ebrahimi

16:15 - 17:00: Keynote #1 - Trust dependable computing for autonomous systems

by Riccardo Locatelli, Intel Corporation

17:05 - 18:05: Session #2 - Reliability issues and reliable designs

- (L) Reliability Evaluation of Digital Channelizers Implemented on SRAM-FPGAs...25 Zhen Gao, Jiajun Xiao and Pedro Revriego
- (L) A Design of Reliable Linear FSMs with Equivalent States in Stochastic Computing...29 Hideyuki Ichihara, Takayuki Fukuda and Tomoo Inoue

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- (S) Mitigation of the impact of across chip systematic process variation using a novel system level design...51 Nabanita Ghoshal, Sree Rama Kc Saraswatula, Santosh Yachareni, Shidong Zhou, Anil Kumar Kandala and Narendra Kumar Pulipati
- ❖ (L) An Aging-Aware CMOS SRAM Structure Design for Boolean Logic In-Memory Computing...55 Wei Chang, Yu-Guang Chen, Po-Yeh Huang and Jin-Fu Li

19:00 to 19:45: Special Session #1 - Industrial best practice: cases of study by automotive chip-makers...59

Organizer/Moderator: Ricardo Cantoro, Politecnico di Torino

- Power characterization of Embedded FLASH memory test...N/A Paolo Bernardi (Politecnico di Torino, IT)
- Software-based self-test development and grading for an AI chip...N/A L. Zaia (Dolphin Design, Fr)
- High-level Fault Injection for Reliability Assessment of Automotive Applications...N/A G. Insinga (Xilinx Inc., US)

DAY 2 - Thursday October 7, 2020

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- (L) Towards Fault Simulation at Mixed Register Transfer/Gate-Level Models...65 Endri Kaja, Nicolas Gerlin, Mounika Vaddeboina, Luis Rivas, Sebastian Prebeck, Zhao Han, Keerthikumara Devarajegowda and Wolfgang Ecker
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- (S) Static Timing Analysis Induced Simulation Errors for Asynchronous Circuits...77 Stavros Simoglou, Nikolaos Blias and Christos Sotiriou

15:35 - 16:20: Keynote #2 – Is Hardware the Next Frontier in Cybersecurity?...N/A by Prof. Ramesh Karri, New York University

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Organizer/Moderator: Emanuele Valea (CEA-List, France)

- Lattice-based cryptography from a hardware perspective...N/A Francesco Regazzoni (University of Amsterdam and Università della Svizzera italiana)
- Introduction to SIKE, plus related fault attack and countermeasure...N/A Simon Pontié (CEA, France)
- Leveraging Inexact Computing in Post-Quantum Cryptography...N/A François-Xavier Standaert (Université Catholique de Louvain)

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- Assessment of side-channel information leakage in cryptographic circuits...N/A Sylvain Guilley (Secure-IC, France)

 Digital sensor dimensioning for mitigating aging-induced reliability concernsN/A
Naghmeh Karimi (UMBC, USA)
18:35: Concluding Session