2021 24th Euromicro Conference on Digital System Design (DSD 2021)

Virtual Conference
1 – 3 September 2021

IEEE Catalog Number: CFP21291-POD
ISBN: 978-1-6654-2704-3

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number: CFP21291-POD
ISBN (Print-On-Demand): 978-1-6654-2704-3
ISBN (Online): 978-1-6654-2703-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

2021 24th Euromicro Conference on Digital System Design (DSD)

DSD 2021

Table of Contents

Message from the General Chair xvii
Message from the DSD Program Chairs xviii
DSD Main Track Program Committee xx
Subreviewers xxv
DSD 2021 Keynotes xxvi

DSD: Digital System Design

Accelerators

A Framework for Hardware-Accelerated Design Space Exploration for Approximate Computing on FPGA 1
Arne Kreddig (SmartRay GmbH, Germany), Simon Conrady (Arnold & Richter Cine Technik, Germany), Manu Manuel (Chair of Integrated Systems, Technical University of Munich, Germany), and Walter Stechele (Chair of Integrated Systems, Technical University of Munich, Germany)

A RISC-V-Based FPGA Overlay to Simplify Embedded Accelerator Deployment 9
Gianluca Bellocchi (University of Modena and Reggio Emilia, Italy), Alessandro Capotondi (University of Modena and Reggio Emilia, Italy), Francesco Conti (University of Bologna, Italy), and Andrea Marongiu (University of Modena and Reggio Emilia, Italy)

A Power-Efficient Parameter Quantization Technique for CNN Accelerators 18
Ercan Kalali (Delft University of Technology, The Netherlands) and Rene Van Leuken (Delft University of Technology, The Netherlands)

Coprocessors

An Efficient FPGA-Based co-Processor for Feature Point Detection and Tracking 24
Toms Stūrmanis (Institute of Electronics and Computer Science, Latvia) and Rihards Novickis (Institute of Electronics and Computer Science, Latvia)

Vector Processing Unit: A RISC-V Based SIMD Co-Processor for Embedded Processing 30
Muhammad Ali (Chair of Adaptive Dynamic Systems, Technische Universität Dresden, Germany), Matthias von Ameln (Chair of Adaptive Dynamic Systems, Technische Universität Dresden, Germany), and Diana Goehringer (Chair of Adaptive Dynamic Systems, Technische Universität Dresden, Germany)

An Open-Source Framework for the Generation of RISC-V Processor + CGRA Accelerator Systems 35
Xiaoyi Ling (University of Toronto), Takahiro Notsu (Fujitsu, Ltd., Japan), and Jason Anderson (University of Toronto)

Video Processing

A Connected Component Labelling Algorithm for a Multi-pixel per Clock Cycle Video Stream .43
Marcin Kowalczyk (AGH University of Science and Technology, Poland) and Tomasz Kryjak (AGH University of Science and Technology, Poland)

An Adaptive Pixel Accumulation Algorithm for a 1D Micro-Scanning LiDAR .51
Ievgeniia Maksymova (Infineon Technologies Austria AG, Austria; Graz University of Technology, Austria), Christian Steger (Graz University of Technology, Austria), and Norbert Druml (Infineon Technologies Austria AG, Austria)

Managing the Resource Continuum in a Real Video Surveillance Scenario .58
Filippo Sciamanna (DEIB, Politecnico di Milano), Michele Zanella (DEIB, Politecnico di Milano), Giuseppe Massari (DEIB, Politecnico di Milano), and William Fornaciari (DEIB, Politecnico di Milano)

Synthesys

A Boolean Heuristic for Disjoint SOP Synthesis .62
Padmanabhan Balasubramanian (Nanyang Technological University, Singapore), Anna Bernasconi (Universita di Pisa, Italy), Valentina Ciriani (Universita degli Studi di Milano, Italy), and Tiziano Villa (Universita degli Studi di Verona, Italy)

Resynthesis of Logic Circuits using Machine Learning and Reconvergent Paths .69
Jitka Kocnová (Brno University of Technology, Czech Republic) and Zdenek Vasicek (Brno University of Technology, Czech Republic)

Decomposition of Transition Systems Into Sets of Synchronizing State Machines .77
Viktor Teren (Università degli Studi di Verona, Italy), Jordi Cortadella (Universitat Politècnica de Catalunya, Spain), and Tiziano Villa (Università degli Studi di Verona, Italy)

Efficient Implementation of Heterogeneous Dataflow Models using Synchronous IO Patterns .82
Omair Rafique (University of Kaiserslautern, Germany), Yu Bai (Hebei University of Science and Technology, China), Klaus Schneider (University of Kaiserslautern, Germany), and Guangxi Yan (Central South University, China)

FPGA Applications

Massively Parallel Binary Neural Network Inference for Detecting Ships in FPGA Systems on the edge .90
Tadej Murovič (ON Semiconductor Adria, Slovenia) and Andrej Trost (University of Ljubljana, Slovenia)

Cache-Accel: FPGA Accelerated Cache Simulator with Partially Reconfigurable Prefetcher .97…
Shivani Shah (International Institute of Information Technology Bangalore, India), Vaibhavi Mathur (International Institute of Information Technology Bangalore, India), Sahithi Meenakshi Vutakuru (International Institute of Information Technology Bangalore, India), Kavya Borra (International Institute of Information Technology Bangalore, India), and Nanditha P. Rao (International Institute of Information Technology Bangalore, India)

FPGA-Based Real-Time Monitoring Support for CAN Applications .101……
Alessandro Cilardo (University of Naples Federico II, Italy) and Stefano Mercogliano (University of Naples Federico II, Italy)

Anomalies, Security and Protection

Employing the Concept of Multilevel Security to Generate Access Protection Configurations for Automotive On-Board Networks .107……
Tobias Dörr (Karlsruhe Institute of Technology (KIT), Germany), Timo Sandmann (Karlsruhe Institute of Technology (KIT), Germany), Hannes Mohr (ERNW Enno Rey Netzwerke GmbH, Germany), and Jürgen Becker (Karlsruhe Institute of Technology (KIT), Germany)

Protecting IoT Devices Through a Hardware-Driven Memory Verification .115……
Troya Çağıl Köylü (Delft University of Technology, the Netherlands), Hans Okkerman (Delft University of Technology, the Netherlands), Cezar Rodolfo Wedig Reinbrecht (Delft University of Technology, the Netherlands), Said Hamdioui (Delft University of Technology, the Netherlands), and Mottaqiallah Taouil (Delft University of Technology, the Netherlands)

Comparative Evaluation of Semi-Supervised Anomaly Detection Algorithms on High-Integrity Digital Systems .123……
Gianluca Martino (Hamburg University of Technology, Germany; German Electron Synchrotron, Germany), Arne Gruenhagen (German Electron Synchrotron, Germany; Hamburg University of Applied Sciences, Germany), Julien Branlard (German Electron Synchrotron, Germany), Annika Eichler (German Electron Synchrotron, Germany), Goerschwin Fey (Hamburg University of Technology, Germany), and Holger Schlarb (German Electron Synchrotron, Germany)

Network on Chip

Fast Simulation of a Many-NPU Network-on-Chip for Microarchitectural Design Space Exploration .131……
Jintaek Kang (Seoul National University, South Korea), Changjae Yi (Seoul National University, South Korea), Keonjoo Lee (Seoul National University, South Korea), Seungwook Lee (SAIT, South Korea), Soojung Ryu (T3K, South Korea), and Soonhoi Ha (Seoul National University, South Korea)

Architectural Implementation of a Reconfigurable NoC Design for Multi-applications .139……
Aparna Nair M K (BITS Pilani-Hyderabad Campus, India), P. Veda Bhanu (BITS Pilani-Hyderabad Campus, India), Soumya J (BITS Pilani-Hyderabad Campus, India), and Linga Reddy Cenkeramaddi (University of Agder, Norway)

Network-on-ReRAM for Scalable Processing-in- Memory Architecture Design .143
Bita Dabiri (University of Tehran, Iran), Mehdi Modarressi (University of Tehran, Iran), and Masoud Daneshtalab (Mälardalen University; Tallinn University of Technology)

Modeling and Simulation - 1

Experimental Evaluation of Statistical Model Checking Methods for Probabilistic Timing Analysis of Multiprocessor Systems .150
Hai-Dang Vu (University of Nantes, France), Sébastien Le Nours (University of Nantes, France), and Sébastien Pillement (University of Nantes, France)

Near-Data-Processing Architectures Performance Estimation and Ranking using Machine Learning Predictors .158
Veronia Iskandar (Technische Universitaet Dresden, Germany), Mohamed A. Abd El Ghany (German University in Cairo/ TU Darmstadt Cairo, Egypt/ Darmstadt, Germany), and Diana Goehringer (Technische Universitaet Dresden, Germany)

Towards Machine Learning Support for Embedded System Tests .166
Stefan Scharoba (Brandenburg University of Technology Cottbus-Senftenberg, Germany), Kai-Uwe Basener (Kostal Industrie Elektrik GmbH, Germany), Jens Bielefeldt (Kostal Industrie Elektrik GmbH, Germany), Hans-Werner Wiesbrock (ITPower Solutions GmbH, Germany), and Michael Hübner (Brandenburg University of Technology Cottbus-Senftenberg, Germany)

Applications

High Speed Implementation of the Deformable Shape Tracking Face Alignment Algorithm .174
Nikos Petrellis (University of Peloponnese, Greece), Stavros Zogas (University of Peloponnese, Greece), Panagiotis Christakos (Dept. of Electrical and Computer Engineer University of Peloponnese, Greece), Georgios Keramidas (Aristotle University of Thessaloniki, Greece), Panagiotis Mousouliotis (Aristotle University of Thessaloniki, Greece), Nikolaos Voros (University of Peloponnese, Greece), and Christos Antonopoulos (University of Peloponnese, Greece)

Highly Parallel Sample Rate Converter for Space Telemetry Transmitters .178
Matteo Bertolucci (University of Pisa) and Luca Fanucci (University of Pisa)

Single-Frame Direct Reflectance Estimation with Indirect Time-of-Flight Cameras .182
Caterina Nahler (Graz University of Technology, Austria), Armin Schoenlieb (Graz University of Technology, Austria), Sebastian Handel (Infineon Technologies Austria AG, Austria), Hannes Plank (Infineon Technologies Austria AG, Austria), Christian Steger (Graz University of Technology, Austria), and Norbert Druml (Infineon Technologies Austria AG, Austria)

Evaluation of Time Series Clustering on Embedded Sensor Platform .187
Wenyao Zhu (KTH Royal Institute of Technology, Sweden) and Zhonghai Lu (KTH Royal Institute of Technology, Sweden)

HW-SW Codesign and Reconfigurability

An Investigation of Dynamic Partial Reconfiguration Offloading in Hard Real-Time Systems .192
Gabriella D'Andrea (Università degli Studi dell'Aquila, Italy), Giacomo Valente (Università degli Studi dell'Aquila, Italy), Luigi Pomante (Università degli Studi dell'Aquila, Italy), and Tania Di Mascio (Università degli Studi dell'Aquila, Italy)

A Hardware/Software Concept for Partial Logic Updates of Embedded Soft Processors at Runtime .199
Tobias Scheipel (Graz University of Technology, Austria), Peter Brungs (University of Würzburg, Germany), and Marcel Baunach (Graz University of Technology, Austria)

Metrics for the Evaluation of Approximate Sequential Streaming Circuits .208
Swantje Plambeck (Hamburg University of Technology, Germany), Gianluca Martino (Hamburg University of Technology, Germany), and Goerschwin Fey (Hamburg University of Technology, Germany)

Frameworks

A Deployment Framework for Quality-Sensitive Applications in Resource-Constrained Dynamic Environments .212
Shayan Tabatabaei Nikkhah (Eindhoven University of Technology, the Netherlands), Marc Geilen (Eindhoven University of Technology, the Netherlands), Dip Goswami (Eindhoven University of Technology, the Netherlands), Martijn Koedam (Eindhoven University of Technology, the Netherlands), Andrew Nelson (Eindhoven University of Technology, the Netherlands), and Kees Goossens (Eindhoven University of Technology, the Netherlands)

ParalOS: A Scheduling & Memory Management Framework for Heterogeneous VPUs .221
Evangelos Petrongonas (National Technical University of Athens, Greece), Vasileios Leon (National Technical University of Athens, Greece), George Lentaris (National Technical University of Athens, Greece), and Dimitrios Soudris (National Technical University of Athens, Greece)

Scheduling Persistent and Fully Cooperative Instructions .229
Yu Yang (KTH Royal Institute of Technology, Sweden), Ahmed Hemani (KTH Royal Institute of Technology, Sweden), and Kolin Paul (Indian Institute of Technology Delhi, India)

Modeling and Simulation - 2

To Pin or Not to Pin: Asserting the Scalability of QEMU Parallel Implementation .238
Marie Badaroux (Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, France), Saverio Miroddi (Open Source and Research Program, Ticketsolve, Germany), and Frédéric Pétrot (Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, France)

Gain and Pain of a Reliable Delay Model .246
Jürgen Maier (ECS Group, TU Wien, Vienna)

Heterogeneous Communication Virtualization for Distributed Embedded Applications 251
Thinh H. Pham (University of Bristol), Shanker Shreejith (The University of Dublin), Sebastian Steinhorst (Technical University of Munich), Suhaib A. Fahmy (King Abdullah University of Science and Technology (KAUST), Thuwal, Saudi Arabia), and Samarjit Chakraborty (University of North Carolina at Chapel Hill)

NMPO: Near-Memory Computing Profiling and Offloading 259
Stefano Corda (Eindhoven University of Technology), Madhurya Kumaraswamy (Eindhoven University of Technology), Ahsan Javed Awan (Ericsson Research), Roel Jordans (Eindhoven University of Technology), Akash Kumar (Technische Universität Dresden), and Henk Corporaal (Eindhoven University of Technology)

EPDSD: European Projects in Digital System Design

Programmable Systems for Intelligence in Automobiles (PRYSTINE): Final Results After Year 3 268
Norbert Druml (n/a), Anna Ryabokon (n/a), Rupert Schorn (n/a), Jochen Koszescha (n/a), Kaspars Ozols (n/a), Aleksandrs Levinskis (n/a), Rihards Novickis (n/a), Ethiopia Nigussie (n/a), Jouni Isoaho (n/a), Selim Solmaz (n/a), Georg Stettinger (n/a), Sergio Diaz (n/a), Mauricio Marcano (n/a), Jorge Villagra (n/a), Juan Medina (n/a), Martina Schwarz (n/a), Antonio Artunedo (n/a), Mauro Comi (n/a), Rutger Beekelaar (n/a), Onur Ozcelik (n/a), Elif Aksu Tasdelen (n/a), Yesim Gurbuz (n/a), Jan Saijets (n/a), Jukka Kyynarainen (n/a), Dmitry Morits (n/a), Bjorn Debaillie (n/a), Maxim Rykunov (n/a), Joan Escamilla (n/a), Jarno Vanne (n/a), Tomi Korhonen (n/a), Kalle Holma (n/a), Eva-Maria Matzhold (n/a), Carlo Novara (n/a), Fabio Tango (n/a), Paolo Burgio (n/a), Giuseppe Calafiore (n/a), Milad Karimshoushtari (n/a), Emilie Boulay (n/a), Miguel Dhaens (n/a), Kylian Praet (n/a), Han Zwijnenberg (n/a), Henri Palm (n/a), David Aledo Ortega (n/a), Ercan Kalali (n/a), Tuomas Pensala (n/a), Arto Kyytinen (n/a), Morten Larsen (n/a), Omar Veledar (n/a), Georg Macher (n/a), Michael Lafer (n/a), Lorenzo Giraudi (n/a), Jakob Reckenzaun (n/a), Daniel Hammer (n/a), Naveen Mohan (n/a), Josef Schmid (n/a), Alfred Hös (n/a), Shai Ophir (n/a), Anand Dubey (n/a), Jonas Fuchs (n/a), Maximilian Lubke (n/a), Andrei Anghel (n/a), Nicolae-Catalin Ristea (n/a), Martin Torngren (n/a), Alua Musralina (n/a), Marlene Harter (n/a), Joseena Memadathil Jose (n/a), and George Dimitrakopoulos (n/a)

Building Blocks and Interaction Patterns of Unmanned Aerial Systems 278
Mahmoud Hussein (Université Paris-Saclay, France; Menofia University, Egypt) and Réda Nouacer (Université Paris-Saclay, France)

TEXTAROSSA: Towards EXtreme Scale Technologies and Accelerators for euROhpc hw/Sw Supercomputing Applications for Exascale ..286
Giovanni Agosta (Politecnico di Milano, DEIB, Italy), Daniele Cattaneo (Politecnico di Milano, DEIB, Italy), William Fornaciari (Politecnico di Milano, DEIB, Italy), Andrea Galimberti (Politecnico di Milano, DEIB, Italy), Giuseppe Massari (Politecnico di Milano, DEIB, Italy), Federico Reghenzani (Politecnico di Milano, DEIB, Italy), Federico Terraneo (Politecnico di Milano, DEIB, Italy), Davide Zoni (Politecnico di Milano, DEIB, Italy), Carlo Brandolese (Politecnico di Milano, DEIB, Italy), Massimo Celino (ENEA, Italy), Francesco Iannone (ENEA, Italy), Paolo Palazzari (ENEA, Italy), Giuseppe Zummo (ENEA, Italy), Massimo Bernaschi (Istituto per le Applicazioni del Calcolo (IAC) - CNR, Italy), Pasqua D'Ambra (Istituto per le Applicazioni del Calcolo (IAC) - CNR, Italy), Sergio Saponara (Università di Pisa, Italy), Marco Danelutto (Università di Pisa, Italy), Massimo Torquati (Università di Pisa, Italy), Marco Aldinucci (Università di Torino, Italy), Yasir Arafat (Università di Torino, Italy), Barbara Cantalupo (Università di Torino, Italy), Iacopo Colonnelli (Università di Torino, Italy), Roberto Esposito (Università di Torino, Italy), Alberto R. Martinelli (Università di Torino, Italy), Gianluca Mittone (Università di Torino, Italy), Olivier Beaumont (INRIA, France), Berenger Bramas (INRIA, France), Lionel Eyraud-Dubois (INRIA, France), Brice Goglin (INRIA, France), Abdou Guermouche (INRIA, France), Raymond Namyst (INRIA, France), Samuel Thibault (INRIA, France), Antonio Filgueras (BSC, Spain), Miguel Vidal (BSC, Spain), Carlos Alvarez (BSC, Spain), Xavier Martorell (BSC, Spain), Ariel Oleksiak (PSNC, Poland), Michal Kulczewski (PSNC, Poland), Alessandro Leonardo (INFN Sezione di Roma, Italy), Piero Vicini (INFN Sezione di Roma, Italy), Francesco Lo Cicero (INFN Sezione di Roma, Italy), Francesco Simula (INFN Sezione di Roma, Italy), Andrea Biagioni (INFN Sezione di Roma, Italy), Paolo Cretaro (INFN Sezione di Roma, Italy), Ottorino Frezza (INFN Sezione di Roma, Italy), Pier Stanislao Paolucci (INFN Sezione di Roma, Italy), Matteo Turisini (INFN Sezione di Roma, Italy), Francesco Giacomini (INFN CNAF, Italy), Tommaso Boccali (INFN Sezione di Pisa, Italy), Simone Montangero (University of Padova and INFN Sezione di Padova, Italy), and Roberto Ammendola (INFN Sezione di Roma Tor Vergata, Italy)

Going to the Edge - Bringing Internet of Things and Artificial Intelligence Together ..295
Michael Karner (Virtual Vehicle Research GmbH, Austria), Joachim Hillebrand (Virtual Vehicle Research GmbH, Austria), Manuela Klocker (Virtual Vehicle Research GmbH, Austria), and Ramiro Samano-Robles (CISTER Research Centre, Portugal)

AIDOaRt: AI-Augmented Automation for DevOps, a Model-Based Framework for Continuous Development in Cyber-Physical Systems ..303
Romina Eramo (University of L'Aquila, Italy), Vittoriano Muttillo (University of L'Aquila, Italy), Luca Berardinelli (Johannes Kepler University, Austria), Hugo Bruneliere (IMT Atlantique, France), Abel Gomez (Universitat Oberta de Catalunya, Spain), Alessandra Bagnato (Softeam, France), Andrey Sadovykh (Softeam, France), and Antonio Cicchetti (Mälardalen University, Sweden)

The H2020-ECSEL Project "iRel40" (Intelligent Reliability 4.0) 311
Klaus Pressel (Infineon Technologies AG, Germany), Josef Moser (Infineon Technologies Austria AG, Austria), Sven Rzepka (Fraunhofer Research Institute for Electronic Nano Systems, Germany), Klas Brinkfeldt (Rise IVF AB, Sweden), Susan Zhao (Signify, Netherlands), Willem van Driel (Signify, Netherlands), Paolo Giammatteo (Università degli Studi dell'Aquila - DEWS, Italy), Barış Bulut (Enforma Bilişim A.Ş., Turkey), Mujdat Soyturk (Marmara University, Turkey), and Luigi Pomante (Università degli Studi dell'Aquila - DEWS, Italy)

Pre-Integrated Architectures for Sustainable Complex Cyber-Physical Systems 319
P. Gougeon (Valeo Comfort and Driving Assistance, France), T. Goubier (Université Paris-Saclay CEA-LIST, France), K. Nguyen (Valeo Comfort and Driving Assistance, France), and T. Arvieu (2IA Consulting, France)

AHSA: Architecture and Hardware for Security Applications

RSM Protection of the PRESENT Lightweight Cipher as a RISC-V Extension 325
Etienne Tehrani (LTCI, Télécom Paris, Institut Polytechnique de Paris, France), Tarik Graba (LTCI, Télécom Paris, Institut Polytechnique de Paris, France), Abdelmalek Si Merabet (LTCI, Télécom Paris, Institut Polytechnique de Paris, France), and Jean-Luc Danger (LTCI, Télécom Paris, Institut Polytechnique de Paris, France)

Secure and Dependable: Area-Efficient Masked and Fault-Tolerant Architectures 333
Vojtěch Miškovský (Czech Technical University in Prague, Czech Republic), Hana Kubátová (Czech Technical University in Prague, Czech Republic), and Martin Novotný (Czech Technical University in Prague, Czech Republic)

Studying OpenCL-Based Number Theoretic Transform for Heterogeneous Platforms 339
Evangelos Haleplidis (Industrial Systems Institute, R.C. ATHENA, Greece; University of Piraeus, Greece), Thanasis Tsakoulis (Industrial Systems Institute, R.C. ATHENA, Greece; University of Patras), Alexander El-Kady (Industrial Systems Institute, R.C. ATHENA, Greece; University of Patras), Charis Dimopoulos (Industrial Systems Institute, R.C. ATHENA, Greece; University of Patras), Odysseas Koufopavlou (University of Patras;), and Apostolos P. Fournaris (Industrial Systems Institute, R.C. ATHENA, Greece)

Novel Non-Cryptographic Hash Functions for Networking and Security Applications on FPGA 347
Thomas Claesen (KU Leuven and Hasselt University, Belgium), Arish Sateesan (KU Leuven, Belgium), Jo Vliegen (KU Leuven, Belgium), and Nele Mentens (imec-COSIC/ES&S, ESAT KU Leuven, Belgium; Leiden University, The Netherlands)

MaDMAN: Detection of Software Attacks Targeting Hardware Vulnerabilities 355
Nikolaos-Foivos Polychronou (Univ. Grenoble Alpes, CEA, LETI, LSOSP, France), Pierre-Henri Thevenon (Univ. Grenoble Alpes, CEA, LETI, LSOSP, France), Maxime Puys (Univ. Grenoble Alpes, CEA, LETI, LSOSP, France), and Vincent Beroulle (Univ. Grenoble Alpes, Grenoble INP, LCIS, France)

Analysis of a Laser-Induced Instructions Replay Fault Model in a 32-bit Microcontroller 363
Vanthanh Khuat (LTCI, Télécom Paris, Institut polytechnique de Paris, France), Jean-Max Dutertre (Mines Saint-Etienne, CEA, Leti, Centre CMP, France), and Jean-Luc Danger (LTCI, Télécom Paris, Institut polytechnique de Paris, France)

Optical Fault Injection Attacks Against Radiation-Hard Shift Registers 371
Dmytro Petryk (IHP – Leibniz-Institut für innovative Mikroelektronik, Germany), Zoya Dyka (IHP – Leibniz-Institut für innovative Mikroelektronik, Germany), Roland Sorge (IHP – Leibniz-Institut für innovative Mikroelektronik, Germany), Jan Schäffner (IHP – Leibniz-Institut für innovative Mikroelektronik, Germany), and Peter Langendörfer (IHP – Leibniz-Institut für innovative Mikroelektronik, Germany; BTU Cottbus-Senftenberg, Germany)

Towards a More Flexible IoT SAFE Implementation 376
Dominic Pirker (Graz University of Technology, Austria; Infineon Technologies AG, Austria), Thomas Fischer (Graz University of Technology, Austria; Infineon Technologies AG, Austria), Christoph Reiter (Infineon Technologies AG, Austria), Harald Witschnig (Infineon Technologies AG, Austria), and Christian Steger (Graz University of Technology, Austria)

5G Security: FPGA Implementation of SNOW-V Stream Cipher 381
Lampros Pyrgas (Industrial Systems Institute of "Athena" RIC in ICT and Knowledge Technologies, Greece; University of the Peloponnese, Greece) and Paris Kitsos (Industrial Systems Institute of "Athena" RIC in ICT and Knowledge Technologies, Greece; University of the Peloponnese, Greece)

Extending Circuit Design Flow for Early Assessment of Fault Attack Vulnerabilities 385
Felipe Valencia (Firmware and Security for Connected Devices, CSEM, Switzerland), Ilia Polian (University of Stuttgart, Germany), and Francesco Regazzoni (University of Amsterdam. ALaRI - USI, The Netherlands)

ITS: Intelligent Transportation Systems

Checkpointing Period Optimization of Distributed Fail-Operational Automotive Applications 389
Philipp Weiss (Technical University of Munich, Germany), Emil Daporta (Technical University of Munich, Germany), Andreas Weichslgartner (AUDI AG, Germany), and Sebastian Steinhorst (Technical University of Munich, Germany)

MPC-Based Speed Tracking for Automated Urban Buses Performing V2I Communications with Traffic Lights 396
Jose A. Matute (TECNALIA, Basque Research and Technology Alliance (BRTA); University of the Basque Country, Spain), Myriam Vaca-Recalde (TECNALIA, Basque Research and Technology Alliance (BRTA); University of the Basque Country, Spain), and Joshue Perez (TECNALIA, Basque Research and Technology Alliance (BRTA))

Controlled Intra-Platoon Collisions for Emergency Braking in Close-Distance Driving Arrangements 402
Dharshan Krishna Murthy (TU Chemnitz, Germany) and Alejandro Masrur (TU Chemnitz, Germany)

Measuring Trust in Automated Driving using a Multi-Level Approach to Human Factors .410.
Philipp Clement (AVL List GmbH, Austria), Herbert Danzinger (AVL List GmbH, Austria), Omar Veledar (AVL List GmbH, Austria), Clemens Könczöl (University of Graz, Austria), Georg Macher (Graz University of Technology, Austria), and Arno Eichberger (Graz University of Technology, Austria)

Runnable Configuration in Mixed Classic/Adaptive AUTOSAR Systems by Leveraging Nondeterminism .418.....
Milan Copic (RWTH Aachen University, Germany), Rainer Leupers (RWTH Aachen University, Germany), and Gerd Ascheid (RWTH Aachen University, Germany)

Enabling Unit Testing of Already-Integrated AI Software Systems: The Case of Apollo for Autonomous Driving .426.....
Miguel Alcon (Universitat Politècnica de Catalunya, Barcelona Supercomputing Center, Spain), Hamid Tabani (Barcelona Supercomputing Center, Spain), Jaume Abella (Barcelona Supercomputing Center, Spain), and Francisco J. Cazorla (Barcelona Supercomputing Center, Spain)

AAMTM: Applications, Architectures, Methods and Tools for Machine - and Deep Learning

TRe-Map: Towards Reducing the Overheads of Fault-Aware Retraining of Deep Neural Networks by Merging Fault Map .434.....
Le-Ha Hoang (Vienna University of Technology (TU Wien)), Muhammad Abdullah Hanif (Vienna University of Technology (TU Wien)), and Muhammad Shafique (New York University Abu Dhabi (NYUAD))

POMMEL: Exploring Off-Chip Memory Energy & Power Consumption in Convolutional Neural Network Accelerators .442.....
Alexander Montgomerie-Corcoran (Imperial College London, UK) and Christos-Savvas Bouganis (Imperial College London, UK)

Improving the Efficiency of Transformers for Resource-Constrained Devices .449.....
Hamid Tabani (Navinfo Europe B.V., The Netherlands), Ajay Balasubramaniam (Navinfo Europe B.V., The Netherlands), Shabbir Marzban (Navinfo Europe B.V., The Netherlands), Elahe Arani (Navinfo Europe B.V., The Netherlands), and Bahram Zonooz (Navinfo Europe B.V., The Netherlands)

Co-Designing Intelligent Control of Building HVACs and Microgrids .457.....
Rumia Masburah (Indian Institute of Technology Kharagpur), Sayan Sinha (Indian Institute of Technology Kharagpur), Rajib Lochan Jana (Indian Institute of Technology Kharagpur), Dr. Soumyajit Dey (Indian Institute of Technology Kharagpur), and Qi Zhu (Northwestern University)

ASHWPA: Advanced Systems in Healthcare, Wellness and Personal Assistance

Model-Based System Architecture for Event-Triggered Wireless Control of Bio-Analytical Devices .465.....
Kanwal Ashraf (Tallinn University of Technology, Estonia), Yannick Le Moullec (Tallinn University of Technology, Estonia), Tamás Pardy (Tallinn University of Technology, Estonia), and Toomas Rang (Tallinn University of Technology, Estonia)

Modeling Battery SoC Predictions for Smart Connected Glasses Simulations 472
Alexis Arcaya Jordan (Université Cote d'Azur, France; Ellcie-Healthy, France), Alain Pegatoquet (Université Cote d'Azur, France), and Andrea Castagnetti (Université Cote d'Azur, France)

Oxygen Saturation Measurement using Hyperspectral Imaging Targeting Real-Time Monitoring 480
Beatriz Martinez-Vega (Universidad de Las Palmas de Gran Canaria, Spain), Raquel Leon (Universidad de Las Palmas de Gran Canaria, Spain), Himar Fabelo (Universidad de Las Palmas de Gran Canaria, Spain), Samuel Ortega (Universidad de Las Palmas de Gran Canaria, Spain), Gustavo M. Callico (Universidad de Las Palmas de Gran Canaria, Spain), David Suarez-Vega (Research Unit and Chronic Pain Unit Hospital Universitario de Gran Canaria Doctor Negrín, Spain), and Bernardino Clavo (Research Unit and Chronic Pain Unit Hospital Universitario de Gran Canaria Doctor Negrín, Spain)

FTET: Future Trends in Emerging Technologies

Design for Restricted-Area and Fast Dilution using Programmable Microfluidic Device Based Lab-on-a-Chip 488
Shuaijie Ying (Ritsumeikan University, Japan), Sudip Roy (IIT Roorkee, India), Juinn-Dar Huang (National Chiao Tung University, Taiwan), and Shigeru Yamashita (Ritsumeikan University, Japan)

Combining SWAPs and Remote CNOT Gates for Quantum Circuit Transformation 495
Philipp Niemann (University of Bremen, Germany; Cyber-Physical Systems, DFKI GmbH, Germany), Luca Mueller (University of Bremen, Germany), and Rolf Drechsler (Universität Bremen, Germany; Cyber-Physical Systems, DFKI GmbH, Germany)

SPCPS: Security and Privacy of Cyber-Physical Systems

Towards Post-Quantum Enhanced Identity-Based Encryption 502
Dariia Verchyk (Technical University of Munich, Germany) and Johanna Sepúlveda (Technical University of Munich, Germany; AIRBUS Defence and Space GmbH, Germany)

Digital Forensics, Video Forgery Recognition, for Cybersecurity Systems 510
Ioannis Memos Bagkratsas (Open University of Cyprus) and Nicolas Sklavos (University of Patras)

Revealing the Secrets of Spiking Neural Networks: The Case of Izhikevich Neuron 514
Luíza C. Garaffa (Delft University of Technology, The Netherlands), Abdullah Aljuffri (Delft University of Technology, The Netherlands), Cezar Reinbrecht (Delft University of Technology, The Netherlands), Said Hamdioui (Delft University of Technlogy, The Netherlands), Mottaqiallah Taouil (Delft University of Technology, The Netherlands), and Johanna Sepulveda (Airbus Defense and Space, Germany)

DTFT: Dependability, Testing and Fault Tolerance in Digital Systems

Automated Debugging-Aware Visualization Technique for SystemC HLS Designs 519
Mehran Goli (University of Bremen/DFKI, Germany; University of Bremen, Germany), Alireza Mahzoon (University of Bremen, Germany), and Rolf Drechsler (University of Bremen/DFKI, Germany; University of Bremen, Germany)

Search Strategy of Large Nonlinear Block Codes 527
Ondrej Novak (Technical University in Liberec, Czech Republic)

Maximizing the Switching Activity of Different Modules Within a Processor Core via Evolutionary Techniques 535
Nikolaos I. Deligiannis (Politecnico di Torino, Italy), Riccardo Cantoro (Politecnico di Torino, Italy), and Matteo Sonza Reorda (Politecnico di Torino, Italy)

An Automated Setup for Large-Scale Simulation-Based Fault-Injection Experiments on Asynchronous Digital Circuits 541
Behal Patrick (Institute for Computer Engineering, TU Wien, Vienna, Austria), Huemer Florian (Institute for Computer Engineering, TU Wien, Vienna, Austria), Najvirt Robert (Institute for Computer Engineering, TU Wien, Vienna, Austria), and Steininger Andreas (Institute for Computer Engineering, TU Wien, Vienna, Austria)

Automatic Design of Fault-Tolerant Systems for VHDL and SRAM-Based FPGAs 549
Jakub Lojda (Brno University of Technology, Czech Republic), Richard Panek (Brno University of Technology, Czech Republic), and Zdenek Kotasek (Brno University of Technology, Czech Republic)

Reliability Analysis of the FPGA Control System with Reconfiguration Hardening 553
Richard Panek (Brno University of Technology, Czech Republic), Jakub Lojda (Brno University of Technology, Czech Republic), Jakub Podivinsky (Brno University of Technology, Czech Republic), and Zdenek Kotasek (Brno University of Technology, Czech Republic)

Implementation-Independent Test Generation for a Large Class of Faults in RISC Processor Modules 557
Maksim Jenihhin (Tallinn University of Technology), Adeboye Stephen Oyeniran (Tallinn University of Technology), Jaan Raik (Tallinn University of Technology), and Raimund Ubar (Tallinn University of Technology)

Author Index 563