2021 34th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI 2021)

Campinas, Brazil
23 – 27 August 2021

IEEE

IEEE Catalog Number: CFP21237-POD
ISBN: 978-1-6654-2171-3

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number: CFP21237-POD
ISBN (Print-On-Demand): 978-1-6654-2171-3
ISBN (Online): 978-1-6654-2170-6

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

Keynotes

David Patterson
University of California at Berkeley and Google, USA

Abstract: Google deployed several TPU generations since 2015, teaching us lessons that changed our views: semiconductor technology advances unequally; compiler compatibility trumps binary compatibility, especially for VLIW domain specific architectures; target total cost of ownership vs initial cost; support multi-tenancy; expect rapid deep neural network (DNN) growth; DNN advances evolve workloads; some inference tasks require floating point; and backwards ML compatibility helps deploy DNNs quickly and tunes them to the TPU. TPUv4i, deployed in 2020, was molded by these lessons.

Naoto Horiguchi
Imec, Leuven, Belgium

Abstract: Recent CMOS scaling is driven by cell height scaling with reducing number of metal lines/standard cell and slow pitch scaling. For the cell height scaling with slow pitch scaling, number of fins/device must be reduced, which causes low drive current and large variability in FinFETs. Nanosheet architectures, such as nanosheet, forksheet and complementary FET (CFET), are proposed to overcome the FinFET issues. Nanosheet architectures enable wider effective transistor width and good electrostatics by stacked nanosheet channels. To scale nanosheet further, atomic channel devices by using 2D materials, such as MoS2 and WSe2, are attractive. Atomic channel devices scale contacted poly pitch beyond Si-based nanosheet devices thanks to good electrostatics by ultra-thin channel. In this presentation, we will discuss challenges and opportunities for nanosheet and atomic channel devices in CMOS scaling.

Rolf Drechsler
University of Bremen at Germany and Director of the Cyber-Physical Systems Group at the German Research Center for Artificial Intelligence (Bremen)

Abstract: Verification is one of the central tasks in circuit and system design. Since the components are used in several safety critical applications, functional correctness has to be ensured. But due to the increasing complexity, complete verification can often not be ensured. As a result, modern verification approaches have to cope with limited resources available, like time or computational power of available machines. Analogously to edge computing, resources constraint computing has to be considered in the context of verification, called Edge Verification in the following. Concepts are presented that allow efficient verification. This might be either by Self-Verification, where the verification hardware is included in the fabricated device, or by Polynomial Verification, where the synthesis process is restricted to guarantee that the generated circuit can be verified in polynomial time. For the later one, a case study is given for efficient polynomial formal verification of totally symmetric functions with short delay.

SBCCI Table of Contents

Session 1 - Analog Design and Applications

Session Chair: Dalton Colombo (UFMG)

Session 2 - Neural Networks

Session Chair: Leandro Mateus Giacomini Rocha (IFRS)

Session 3- Analog Design for Low Power

Session Chair: Pietro Ferreira (Université Paris-Saclay)

Session 4 - Video Coding

Session Chair: César Augusto Missio Marcon (PUCRS)

Session 5 - Many-core Systems

Session Chair: Mônica Magalhães Pereira (UFRN)

Session 6 - Design Automation and Reliability

Session Chair: José Luís Güntzel (UFSC)

Session 7 - Digital Design for Low Power - Circuits

Session Chair: Leonardo Bandeira Soares (IFRS)

Session 8 - Digital Design for Low Power - Architectures

Session Chair: Fábio Luís Livi Ramos (UNIPAMPA)

Session 9 - Quantum Computing and New Devices

Session Chair: Omar Paranaiba Vilela Neto (UFMG)