

# **2021 34th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI 2021)**

**Campinas, Brazil  
23 – 27 August 2021**



**IEEE Catalog Number: CFP21237-POD  
ISBN: 978-1-6654-2171-3**

**Copyright © 2021 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP21237-POD
ISBN (Print-On-Demand):	978-1-6654-2171-3
ISBN (Online):	978-1-6654-2170-6

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# Keynotes

David Patterson

University of California at Berkeley and Google, USA

Ten Lessons from Three Generations Shaped Google's TPUv4i.....**N/A**

**Abstract:** Google deployed several TPU generations since 2015, teaching us lessons that changed our views: semiconductor technology advances unequally; compiler compatibility trumps binary compatibility, especially for VLIW domain specific architectures; target total cost of ownership vs initial cost; support multi-tenancy; expect rapid deep neural network (DNN) growth; DNN advances evolve workloads; some inference tasks require floating point; and backwards ML compatibility helps deploy DNNs quickly and tunes them to the TPU. TPUv4i, deployed in 2020, was molded by these lessons.

Naoto Horiguchi

Imec, Leuven, Belgium

CMOS device architecture evolution from FinFETs to nanosheet and atomic channel devices.....**N/A**

**Abstract:** Recent CMOS scaling is driven by cell height scaling with reducing number of metal lines/standard cell and slow pitch scaling. For the cell height scaling with slow pitch scaling, number of fins/device must be reduced, which causes low drive current and large variability in FinFETs. Nanosheet architectures, such as nanosheet, forksheet and complementary FET (CFET), are proposed to overcome the FinFET issues. Nanosheet architectures enable wider effective transistor width and good electrostatics by stacked nanosheet channels. To scale nanosheet further, atomic channel devices by using 2D materials, such as MoS<sub>2</sub> and WSe<sub>2</sub>, are attractive. Atomic channel devices scale contacted poly pitch beyond Si-based nanosheet devices thanks to good electrostatics by ultra-thin channel. In this presentation, we will discuss challenges and opportunities for nanosheet and atomic channel devices in CMOS scaling.

Rolf Drechsler

University of Bremen at Germany and Director of the Cyber-Physical Systems Group at the German Research Center for Artificial Intelligence (Bremen)

Edge Verification: Ensuring Correctness under Resource Constraints.....**1**

**Abstract:** Verification is one of the central tasks in circuit and system design. Since the components are used in several safety critical applications, functional correctness has to be ensured. But due to the increasing complexity, complete verification can often not be ensured. As a result, modern verification approaches have to cope with limited resources available, like time or computational power of available machines. Analogously to edge computing, resources constraint computing has to be considered in the context of verification, called Edge Verification in the following. Concepts are presented that allow efficient verification. This might be either by Self-Verification, where the verification hardware is included in the fabricated device, or by Polynomial Verification, where the synthesis process is restricted to guarantee that the generated circuit can be verified in polynomial time. For the later one, a case study is given for efficient polynomial formal verification of totally symmetric functions with short delay.

# SBCCI Table of Contents

## Session 1 - Analog Design and Applications

Session Chair: Dalton Colombo (UFMG)

<b>A Latching Current Limiter with Telemetries for Space Applications.....7</b> Ronald Hassib Galvis Chacón, Agnaldo Vieira Dias, Ângela Alves dos Santos, Paula Cristiane Secheusk, Silvio Manea, José Alexandre Diniz and Saulo Finco <b>CTI, INPE, UNICAMP</b>
<b>Injection-Locked Ring Oscillator based Phase Locked Loop For 1.6 Gbps Clock Recovery.....13</b> Dorian Vert, Michel PIGNOL, Vincent LEBRE, Emmanuel MOUTAYE, Florence MALOU and Jean-Baptiste Begueret <b>University of Bordeaux, Centre National d'Etudes Spatiales (CNES), Thales Alenia Space (France)</b>
<b>A 237 ppm/°C L-Band Active Inductance Based Voltage Controlled Oscillator in SOI 0.18 <math>\mu\text{m}</math>.....18</b> João Roberto Raposo de Oliveira Martins, Francisco Alves and Pietro Maris Ferreira <b>Université Paris-Saclay (France)</b>
<b>Modeling of Reconfigurable <math>\Sigma\Delta</math> Modulator for Multi-standard Wireless Receivers in Verilog-A.....24</b> Mateus Castro, Raphael Noal Souza, Agord Junior, Eduardo Lima and Leandro Manera <b>UNICAMP, Instituto de Pesquisas Eldorado</b>
<b>Multifunctional auricular vagus nerve stimulator for closed-loop application.....30</b> Babak Dabiri, Klaus Zeiner, Arnaud Nativel and Eugenijus Kaniusas <b>Institute of Electrodynamics, Microwave and Circuit Engineering (Austria)</b>

## Session 2 - Neural Networks

Session Chair: Leandro Mateus Giacomini Rocha (IFRS)

<b>Machine Learning Models for EDA Application.....N/A</b> Youngsoo Shin <b>KAIST - Korea Advanced Institute of Science and Technology (invited talk)</b>
<b>FLoPAD-GRU: A Flexible, Low Power, Accelerated DSP for Gated Recurrent Unit Neural Network.....35</b> Ilayda Yaman, Allan Andersen, Lucas Ferreira and Joachim Rodrigues <b>Lund University (Sweden)</b>
<b>Exploring Constant Signal Propagation to Optimize Neural Network Circuits.....40</b> Augusto Berndt, Cristina Meinhardt, Paulo Butzen and Andre Reis <b>UFRGS, UFSC</b>
<b>Artificial Neural Network Based Automatic Modulation Classification System Applied to FPGA.....46</b> Adenilson Castro, Ronny Milléo, Luis Lolis and André Mariano <b>UFPR</b>

## Session 3- Analog Design for Low Power

Session Chair: Pietro Ferreira (Université Paris-Saclay)

<b>0.5 V 19 nW Smart Temperature Sensor for Ultra-Low-Power CMOS Applications.....52</b> Daniel Lott and Dalton Colombo <b>UFMG</b>
<b>Exploration of a Low-power CMOS Voltage Squarer.....58</b> Victor Costa, Adilson Cardoso, Cesar Rodrigues, Andre Aita and Jefferson Marques <b>UFSM, UFSC</b>
<b>A 0.6V, 3.3nW, Adjustable Gaussian Circuit for Tunable Kernel Functions.....64</b> Vassilis Alimisis, Marios Gourdouparis, Christos Dimas and Paul Sotiriadis <b>National Technical University of Athens (Greece)</b>  <b>Best Paper Award</b>

## Session 4 - Video Coding

Session Chair: César Augusto Missio Marcon (PUCRS)

<b>High-throughput and low-power architectures for the AV1 Arithmetic Encoder.....70</b> Tulio Pereira Bitencourt, Fábio Luís Livi Ramos and Sergio Bampi <b>UFRGS, UNIPAMPA</b>
<b>High-Performance Design for the AV1 Multi-Alphabet Arithmetic Decoder.....76</b> Jiovana Gomes and Fábio Luís Livi Ramos <b>UNIPAMPA</b>
<b>High-Throughput Sharp Interpolation Filter Hardware Architecture for the AV1 Video Codec.....82</b> Daiane Freitas, Cláudio Diniz, Mateus Grellert and Guilherme Corrêa <b>UFPEL, UFSC, UFRGS</b>
<b>Configurable Power/Quality-Aware Hardware Design for the AV1 Directional Intra Frame Prediction.....88</b> Luiz Neto, Marcel Correa, Bruno Zatt, Daniel Palomino, Luciano Agostini and Guilherme Corra <b>UFPEL</b>
<b>Configurable Approximate Hardware Accelerator to Compute SATD and SAD Metrics for Low Power All Intra High Efficiency Video Coding.....94</b> Victor Lima, Matheus Stigger, Leonardo Bandeira Soares, Cludio Diniz and Sergio Bampi <b>UCPeI, UFRGS</b>

## Session 5 - Many-core Systems

Session Chair: Mônica Magalhães Pereira (UFRN)

<b>Security Aspects of Reconfigurable FPGAs: from embedded to multi-tenant cloud.....N/A</b> Lars Bauer <b>Karlsruhe Institute of Technology (KIT), Germany (invited talk)</b>
<b>MUTECO: A Framework for Collaborative Allocation in CPU-FPGA Multi-tenant Environments.....100</b> Michael Jordan, Guilherme Korol, Mateus Beck Rutzig and Antonio Carlos Schneider Beck <b>UFRGS, UFSM</b>
<b>Management Application - a New Approach to Control Many-Core Systems.....106</b> Angelo Dalzotto, Leonardo Erthal, Marcelo Ruaro and Fernando Moraes <b>PUCRS</b>
<b>Reflect3d: An Adaptive and Fault-Tolerant Routing Algorithm for Vertically-Partially-Connected 3D-NoC.....112</b> Alexandre Almeida da Silva, Leonel Maia e Silva Junior, Alexandre Coelho, Jarbas Silveira and César Marcon <b>UFC, PUCRS</b>

## Session 6 - Design Automation and Reliability

Session Chair: José Luís Güntzel (UFSC)

<b>Accuracy and Size Trade-off of a Cartesian Genetic Programming Flow for Logic Optimization.....118</b> Augusto Berndt, Isac Campos, Brunno Abreu, Bryan Lima, Mateus Grellert, Jônata Carvalho and Cristina Meinhardt <b>UFRGS, UFSC</b>
<b>A method to join the On-set and Off-set of an incompletely boolean function into a single BDD.....124</b> Renato Peralta, João Nespolo, Paulo Butzen, Mariana Kolberg and Andre Reis <b>UFRGS</b>
<b>Asymmetric Aging Avoidance EDA Tool.....130</b> Freddy Gabbay, Avi Mendelson, Basel Salame and Majd Ganaiem <b>Rupp Academic Center and Technion – Israel Institute of Technology (Israel)</b>
<b>A Versatile Test Set Generation Tool for Structural Analog Circuit Testing.....136</b> Lucas Zilch, Marcelo Lubaszewski and Tiago Balen <b>UFRGS</b>

## Session 7 - Digital Design for Low Power - Circuits

Session Chair: Leonardo Bandeira Soares (IFRS)

<b>Exploring Approximate Computing and Near-Threshold Operation to Design Energy-efficient Multipliers.....142</b> Vincius Zanandrea, Douglas Borges, Vagner Rosa and Cristina Meinhardt <b>UFSC, FURG</b>
<b>Optimizing Partial Product Terms for a Power-Efficient Radix-4 Modified Booth Multiplier.....148</b> Jean Scheunemann, Marlon Sigales, Mateus Fonseca and Eduardo Costa <b>UCPel, UFPEL</b>
<b>A Robust and Power-Efficient VLSI Power Line Interference Canceling Design.....154</b> Morgana Macedo Azevedo da Rosa, Patricia da Costa, Guilherme Paim, Eduardo da Costa, Sergio Almeida and Sergio Bampi <b>UCPel, UFRGS</b>
<b>Soft Error Tolerant Quasi-Delay Insensitive Asynchronous Circuits: Advancements and Challenges.....160</b> Ashiq Sakib <b>Florida Polytechnic University (USA)</b>

## Session 8 - Digital Design for Low Power - Architectures

Session Chair: Fábio Luís Livi Ramos (UNIPAMPA)

<b>Application of injection locked relaxation oscillators to the design of ultra-low power sensor interfaces.....N/A</b> Franck BADETS <b>CEA Leti, Département DCOS (invited talk)</b>
<b>Improving energy efficiency by transparently sharing SIMD Execution Units in Asymmetric Multicores.....166</b> Caio Vieira and Antonio Carlos Schneider Beck <b>UFRGS</b>
<b>ETCG: Energy-Aware CPU Thread Throttling for CPU-GPU Collaborative Environments.....172</b> Tiago Knorst, Michael Jordan, Arthur Lorenzon, Mateus Beck Rutzig and Antonio Carlos Schneider Beck <b>UFRGS, UNIPAMPA, UFSM</b>
<b>Evaluating the Performance, Energy and Area Tradeoffs of ATHENA in Superscalar Processors.....178</b> Francisco Carlos Silva Junior, Ricardo Jacobi and Ivan Silva <b>UNB, UFPI</b>

## Session 9 - Quantum Computing and New Devices

Session Chair: Omar Paranaíba Vilela Neto (UFMG)

<b>Modeling wave propagation using automata cellular on Chip.....184</b> Henrique de Moura and Daniel Munoz <b>UNB</b>
<b>Novel Three-Input Gates for Silicon Quantum Dot.....190</b> Maria Dalila Vieira, Icaro Moreira, Pedro Silva, Laysson Luz, Ricardo Ferreira, Omar Vilela Neto and José Augusto Nacif <b>UFV, UFMG</b>
<b>Optimizing a Robust Miller OTA Implemented with Diamond MOSFETs By Using iMTGSPICE.....196</b> José Roberto Banin Júnior, Rodrigo Moreto, Gabriel da Silva, Carlos Thomaz and Salvador Gimenez <b>FEI</b>