

2020 IEEE International Integrated Reliability Workshop (IIRW 2020)

**Virtual Conference
4 October – 1 November 2020**



**IEEE Catalog Number: CFP20IRW-POD
ISBN: 978-1-7281-7059-6**

**Copyright © 2020 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP20IRW-POD
ISBN (Print-On-Demand):	978-1-7281-7059-6
ISBN (Online):	978-1-7281-7058-9
ISSN:	1930-8841

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

IIRW 2020 Table of Contents

IIRW 2020 Committees	v
IIRW 2020 Program Schedule	vii
Call for Papers 2021	xvi
Foreword	xvii
Keynote	xix
Summaries of Invited Papers	xx

Technical Papers

FEOL Self-Heating and BEOL Joule-Heating Effects of FinFET Technology and Its Implications for Reliability Prediction	1
<i>Hai Jiang, Taeyoung Jeong, Hyunchul Sagong, Kihyun Choi, Minjung Jin, Myungsoo Yeo, Hwasung Rhee, and Euncheol Lee</i>	
Accelerated Testing of SiC Power Devices	6
<i>Daniel J. Lichtenwalner, Shadi Sabri, Edward van Brunt, Brett Hull, Sei-Hyung Ryu, Philipp Steinmann, Amy Romero, Satyaki Ganguly, Donald A. Gajewski, Scott Allen, and John W. Palmour</i>	
ON-State Gate Stress Induced Threshold Voltage Instabilities in p-GaN Gate AlGaIn/GaN HEMTs	12
<i>Arno Stockman and Peter Moens</i>	
Plasma Induced Charging Damage: From Appropriate MOS Test Structures to Antenna Design Rules, a Comprehensive Process Qualification Procedure	16
<i>Andreas Martin</i>	
On the Impact of Gate Field-Plate Length and Barrier Layer Thickness on TDDB Lifetime of GaN-on-Si MISHEMT Devices for RF/5G/mm-Wave Applications	24
<i>Chien-Yu Lin, Vamsi Putcha, Alireza Alian, Niamh Waldron, Dimitri Linten, Nadine Collaert, and Ting-Chang Chang</i>	
Modeling the Hysteresis of Current-Voltage Characteristics in 4H-SiC Transistors	31
<i>Alexander Vasilev, Markus Jech, Alexander Grill, Gerhard Rzepa, Christian Schleich, Alexander Makarov, Gregor Pobegen, Tibor Grasser, Michael Waltl, and Stanislav Tyaginov</i>	
Utilizing Acoustic Emission Signals to Evaluate BEoL Stack Damages of Two Different Sample Systems Caused by Cu-Pillar Shear-Off	35
<i>Jendrik Silomon, André Clausner, and Ehrenfried Zschech</i>	
Points-Over-Threshold Statistics for Post-Retention Read Disturb Reliability in 3D NAND Flash	40
<i>Cristian Zambelli, Luca Crippa, Rino Micheloni, and Piero Olivo</i>	
Combining Topological & Physical Pattern Recognition to Enhance Memory Chip Reliability	45
<i>Sherif Hany, Sunsoo Byun, Hossam Sarhan, Dina Medhat, Mohamed ElRefaee, Jaehyun Jang, Baekryong Jeong, Hyunseung Choi, Sunmi Choi, Jonathan Muirhead, and Matthew Hogan</i>	

Circuit Reliability Analysis of In-Memory Inference in Binarized Neural Networks	49
<i>Tommaso Zanotti, Francesco Maria Puglisi, and Paolo Pavan</i>	
Cumulated Charging Mechanisms at Gate Processing in High-κ First Planar NMOS Devices	54
<i>Gaspard Hiblot, Narendra Parihar, Emmanuel Dupuy, Geert Mannaert, Sylvain Baudot, Ben Kaczer, Vincent De Heyn, and Abdelkarim Mercha</i>	
Hierarchical High Sigma Monte Carlo Simulation of SRAM Vmin Shift by Parts for Automotive Grade Fail Rate Projection	58
<i>M. Ahsan ul Karim, S. Balasubramanian, L. Peters, K. Fisher, J. Dyck, Y. Song, M. Luque, J. Higman, and T. Nigam</i>	
Distribution of Step Heights of Electron and Hole Traps in SiON nMOS Transistors	62
<i>K. Tselios, B. Stampfer, J. Michl, E. Ioannidis, H. Enichlmair, and M. Waltl</i>	
Impact of Interface Layer on Charge Trapping in Si:HfO₂ Based FeFET	68
<i>Taehwan Jung, Barry O'Sullivan, Nicolò Ronchi, Dimitri Linten, Changhwan Shin, and Jan Van Houdt</i>	
Regular Posters	
Impact of Atomic Layer Deposition Co-Reactant Pulse Time on 65nm CMOS Integrated Hafnium Dioxide-Based Nanoscale RRAM Devices	74
<i>Jubin Hazra, Maximilian Liehr, Karsten Beckmann, Sarah Rafiq, and Nathaniel Cady</i>	
Charge Pumping and Flicker Noise-Based Defect Characterization in Ferroelectric FETs	78
<i>Yannick Raffel, Maximilian Lederer, Ricardo Olivo, Franz Müller, Raik Hoffmann, Tarek Ali, Thomas Kämpfe, Konrad Seidel, and Johannes Heitmann</i>	
Impact of Switching Variability of 65nm CMOS Integrated Hafnium Dioxide-Based ReRAM Devices on Distinct Level Operations	82
<i>Maximilian Liehr, Jubin Hazra, Karsten Beckmann, Sarah Rafiq, and Nathaniel Cady</i>	
Electrically Detected Magnetic Resonance Study of High-Field Stress Induced Si/SiO₂ Interface Defects	86
<i>Stephen J. Moxim, Patrick M. Lenahan, Fedor V. Sharov, Gaddi S. Haase, and David R. Hughart</i>	
Addressing Weak Links in Automotive Reliability: Semiconductor Contamination Control, Inspection and Test	90
<i>Andreas Aal, Jennifer Braggin, Antoine Amade, and Mark Puttock</i>	
Challenges and Solution Approaches for Simulation-Based Reliability Assessment - Degradation Modeling	94
<i>André Lange and Roland Jancke</i>	
Open Posters	
ANtarctica: ANalog Thermal Aware, with Reduced Constraint, Technique for Checking & Analysis	97
<i>Sherif Hany, Hany Fekri Ragai, and Emad Hegazi</i>	
Summaries of Tutorials	101
Discussion Group Slides	105
Author Index	155