

2020 ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP 2020)

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SLIP^2 2020 FINAL PROGRAM

November 5th, 2020. Co-located with ICCAD 2020.

Time (Pacific Time)	Program
8:30	Welcome, Program Overview, Housekeeping, Keynote Introduction
8:40	Keynote Session 1 — Outlook of device and assembly technologies enabling high performance mobile computing - IRDS view (Invited) (<u>abstract</u>).....1 Mustafa Badaroglu (<i>Qualcomm, Belgium</i>)
9:20	Q&A
9:35	Break
9:45	Paper Session 1 — Interconnect Aspects of Advanced Technologies and Applications (3 x 20 min.) Session Chair: Brian Cline (<i>ARM, USA</i>) <ul style="list-style-type: none">○ Communication architecture enabling 100X accelerated simulation of biological neural networks.....8 Kevin Kauth, Tim Stadtmann, Ruben Brandhofer, Vida Sobhani and Tobias Gemmeke (<i>IDS, RWTH Aachen University, Germany</i>)○ Pathfinding for 2.5D interconnect technologies.....16 Saptadeep Pal and Puneet Gupta (<i>UCLA, USA</i>)○ Global interconnects in VLSI complexity SFQ systems.....24 Tahereh Jabbari and Eby Friedman (<i>University of Rochester, USA</i>)
10:45	Discussants + Q&A <ul style="list-style-type: none">• Louis Scheffer (<i>HHMI, USA</i>)• Sung-Kyu Lim (<i>Georgia Tech, USA</i>)

Time (Pacific Time)	Program
11:00	<p>Invited Session 1 — Quantum Computing (2 x 25 min.) Session Chair: Rasit O. Topaloglu (IBM, USA)</p> <ul style="list-style-type: none"> ○ Building a Quantum Computer (Invited).....31 Barry C. Sanders (<i>University of Calgary, Canada</i>) ○ Extending quantum systems with optical interconnects (Invited).....35 Jason Orcutt (<i>IBM, USA</i>)
11:50	<p>Discussants + Q&A</p> <ul style="list-style-type: none"> • Koen Bertels (<i>QBee, Portugal & University of Porto, Portugal</i>)
12:00	<p>Break / Open Discussion — Problems and Pathfinding Challenges</p>
12:30	<p>Keynote Session 2 — Wafer scale interconnect and pathfinding for machine learning hardware (Invited) (abstract).....36 Patrick Groeneveld (<i>Cerebras Systems, USA</i>)</p>
13:10	<p>Q&A</p>
13:25	<p>Invited Session 2 — NoCs (2 x 25 min.) Session Chair: Dirk Stroobandt (<i>Ghent University, Belgium</i>)</p> <ul style="list-style-type: none"> ○ Analytical Modeling of NoCs for Fast Simulation and Design Exploration (Invited).....37 Raid Ayoub (<i>Intel, USA</i>) ○ Role of on-chip networks in building domain-specific architectures (DSAs) for sparse computations (Invited).....38 Abhishek Jain (<i>Xilinx, USA</i>)

Time (Pacific Time)	Program
14:15	Discussants + Q&A <ul style="list-style-type: none"> • Henri Fraisse (<i>Xilinx, USA</i>) • Paolo D'Alberto (<i>Xilinx, USA</i>)
14:25	Break
14:35	<p>Paper Session 2 — Interconnect Prediction, Analysis and Optimization (3 x 20 min.)</p> <p>Session Chair: Mahesh Iyer (<i>Intel, USA</i>)</p> <ul style="list-style-type: none"> ○ Revisiting inherent noise floors for interconnect prediction.....39 Tuck-Boon Chan (<i>Qualcomm, USA</i>), Andrew B. Kahng (<i>UCSD, USA</i>) and Mingyu Woo (<i>UCSD, USA</i>) ○ 3D NoC emulation model on a single FPGA.....46 Jonathan D'hoore (<i>Ghent University, Belgium</i>), Poona Bahrebar (<i>UC Irvine, USA & Ghent University, Belgium</i>) and Dirk Stroobandt (<i>Ghent University, Belgium</i>) ○ Optimal bounded-skew Steiner trees to minimize maximum k-active dynamic power.....54 Hamed Fatemi (<i>NXP Semiconductors, USA</i>), Andrew B. Kahng (<i>UCSD, USA</i>), Minsoo Kim (<i>UCSD, USA</i>) and Jose Pineda de Gyvez (<i>NXP Semiconductors, USA</i>)
15:35	Discussants + Q&A <ul style="list-style-type: none"> • Patrick Groeneveld (<i>Cerebras Systems, USA</i>) • Rob Aitken (<i>ARM, USA</i>)
15:50	Workshop Closing — Future directions/Community mechanisms