# 2020 International Conference on Simulation of Semiconductor Processes and Devices
# (SISPAD 2020)

Kobe, Japan
23 September – 6 October 2020

IEEE Catalog Number: CFP20SSD-POD
ISBN: 978-1-7281-7354-2

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IEEE Catalog Number: CFP20SSD-POD
ISBN (Print-On-Demand): 978-1-7281-7354-2
ISBN (Online): 978-4-86348-763-5
ISSN: 1946-1569

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# SISPAD 2020 Technical Program

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S. Martinie[1], O. Rozeau[1], T. Poiroux[1], P. Scheer[1], S. E. Ghouli[2], M. Kang[3], A. Juge[2], H. Lee[3]
([1]CEA, LETI, Univ. Grenoble Alpes, France, [2]STMicroelectronics, France,
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"Complementary FET Device and Circuit Level Evaluation Using Fin-Based and Sheet-Based Configurations Targeting 3nm Node and Beyond"
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([1]Applied Materials, India, [2]Applied Materials, U.S.A.) ................................................ 327

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Hiuyung Wong (San Jose State Univ., U.S.A.)

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S. S. Raju[1], B. Wang[2], K. Mehta[1], M. Xiao[2], Y. Zhang[2], H.-Y. Wong[1]
([1]San Jose Univ., U.S.A., [2]Virginia Polytech. Inst. State Univ., U.S.A.)....................351

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([1]Univ. Texas at Dallas, U.S.A., [2]imec, Belgium)....................363

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([1]Kobe Univ., Japan, [2]Panasonic, Japan) ........................................................................367

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([1]National Chaio Tung Univ., Taiwan, [2]Tohoku Univ., Japan) ...........................................375

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