

2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT 2020)

**Hsinchu, Taiwan
10 – 13 August 2020**



**IEEE Catalog Number: CFP20847-POD
ISBN: 978-1-7281-6084-9**

**Copyright © 2020 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP20847-POD
ISBN (Print-On-Demand):	978-1-7281-6084-9
ISBN (Online):	978-1-7281-6083-2
ISSN:	2380-7369

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

A NOISE-SHAPING SAR ASSISTED MASH 2-1 SIGMA-DELTA MODULATOR	1
<i>Yu-Sian Lin, Soon-Jyh Chang, Chia-Ling Wei</i>	
A 12-BIT 100-KS/S SAR ADC FOR IOT APPLICATIONS	5
<i>Yung-Hui Chung, Qi-Feng Zeng</i>	
A CMOS TEMPERATURE SENSOR BASED ON A CHOPPED CONTINUOUS-TIME DELTA-SIGMA MODULATOR.....	9
<i>Po-Yu Li, Wei-En Lee, Ching-Tzung Lin, Li-Te Wu, Tsung-Hsien Lin</i>	
RESISTOR-BASED TEMPERATURE SENSING CHIP WITH DIGITAL OUTPUT	11
<i>Kai-Min Chang, Yen-Ju Lin, Chia-Liang Wei, Soon-Jyh Chang</i>	
FAULT-AWARE ECC TECHNIQUES FOR RELIABILITY ENHANCEMENT OF FLASH MEMORY	15
<i>Shyue-Kung Lu, Zeng-Long Tsai, Chun-Lung Hsu, Chi-Tien Sun</i>	
A COST-EFFECTIVE RELIABLE EDGE COMPUTING HARDWARE DESIGN BASED ON MODULE SIMPLIFICATION AND DUPLICATION: A CASE STUDY ON VEHICLE DETECTION BASED ON SUPPORT VECTOR MACHINE	17
<i>Tong-Yu Hsieh, Hsin-Yung Shen, Chia-Teng Hsu</i>	
RELIABILITY ANALYSIS OF RECONFIGURATION CONTROLLER FOR FPGA-BASED FAULT TOLERANT SYSTEMS: CASE STUDY	21
<i>Richard Panek, Jakub Lojda, Jakub Podivinsky, Zdenek Kotasek</i>	
THE RISE OF RISC-V FROM EDGE TO CLOUD.....	25
<i>Charlie Hong-Men Su</i>	
AI ACCELERATION WITH RISC-V FOR EDGE COMPUTING	26
<i>Chia-Hsiang Yang</i>	
EXPERIMENTS AND OPTIMIZATIONS FOR TVM ON RISC-V ARCHITECTURES WITH P EXTENSION.....	27
<i>Yi-Ru Chen, Hui-Hsin Liao, Chia-Hsuan Chang, Che-Chia Lin, Chao-Lin Lee, Yuan-Ming Chang, Chun-Chieh Yang, Jenq-Kuen Lee</i>	
RFIC AND RF MODULE FOR 5G APPLICATIONS.....	31
<i>Ming-Da Tsai, Song-Yu Yang, Chi-Yao Yu, Ping-Yu Chen, Tzung-Han Wu, Mohammed Hassan, Chi-Tsan Chen, Chao-Wei Wang, Yen-Chuan Huang, Li-Han Huang, Wei-Hao Chiu, Anson Lin, Bo-Yu Lin, Arnaud Werquin, Chien-Cheng Lin, Yen-Horng Chen, Jen-Che Tsai, Yuan-Yu Fu, Bernard Tenbroek, Ching-Shiun Chiu, Yi-Bin Lee, Guang-Kaai Dehng</i>	
DESIGN SOLUTIONS FOR 5G POWER AMPLIFIERS USING 0.15 μ M AND 0.25 μ M GAN HEMTS	34
<i>Yi-Qi Lin, Andrew Patterson</i>	
5G MMWAVE TECHNOLOGY DESIGN CHALLENGES AND DEVELOPMENT TRENDS	37
<i>Wen Chiang Chen</i>	
MINIDEVIATION: AN EFFICIENT MULTI-STAGE BUS-AWARE GLOBAL ROUTER	41
<i>Weida Zhu, Xinghai Zhang, Genggeng Liu, Wenzhong Guo, Ting-Chi Wang</i>	

CORONA: A K-CONNECTED ROBUST INTERCONNECTION NETWORK GENERATION ALGORITHM.....	45
<i>H.-I. Wu, Ren-Song Tsay, Fong-Yuan Chang</i>	
STITCH-AWARE ROUTING CONSIDERING SMART BOUNDARY FOR MULTIPLE E- BEAM LITHOGRAPHY	49
<i>Chih-Hsiang Hsu, Shao-Yun Fang</i>	
AUTOMATIC FLOORPLANNING FOR AI SOCS.....	53
<i>Tai-Chen Chen, Pei-Yu Lee, Tung-Chieh Chen</i>	
DEEP LEARNING CREATIVITY IN EDA	55
<i>Cheng-Kuang Lee</i>	
FAULT-TOLERANCE MECHANISM ANALYSIS ON NVDLA-BASED DESIGN USING OPEN NEURAL NETWORK COMPILER AND QUANTIZATION CALIBRATOR.....	56
<i>Shu-Ming Liu, Luba Tang, Ning-Chi Huang, Der-Yu Tsai, Ming-Xue Yang, Kai-Chiang Wu</i>	
LOW-ACTIVE-ENERGY AND LOW-STANDBY-POWER SUB-THRESHOLD ROM FOR IOT EDGE SENSING SYSTEMS.....	59
<i>Jinn-Shyan Wang, Chien-Tung Liu, Chao-Hsiang Wang</i>	
REAL-TIME ERROR MONITORING SYSTEM CONSIDERING ENDURANCE AND DATA- RETENTION CHARACTERISTICS OF TAOX-BASED RERAM STORAGE WITH WORKLOADS AT DATA CENTERS.....	63
<i>Yoshiki Kakuta, Reika Kinoshita, Hiroshi Kinoshita, Chihiro Matsui, Ken Takeuchi</i>	
EDGE-AI BASED CATTLE BEHAVIOR ESTIMATION SYSTEM FOR GRAZING.....	67
<i>Hiroyuki Ito</i>	
AI IN TRANSPORTATION AND VIDEO INFERENCE SPEEDUP	68
<i>Hung-Hsuan Lin</i>	
COMPUTING-IN-MEMORY A PROCESSING-IN-SENSOR TECHNIQUES FOR LOW- POWER EDGE DEVICES.....	69
<i>Kea-Tiong Tang</i>	
INTELLIGENT DOCUMENT RECOGNITION ON FINANCIAL PROCESS AUTOMATION	70
<i>Wen-Pin Hsu</i>	
CAD FOR SECURITY: A FULL REVERSE ENGINEERING TOOLCHAIN FROM LAYOUT TO RTL.....	71
<i>Yier Jin</i>	
HARDWARE TROJAN DETECTION AT RUN-TIME USING MACHINE-LEARNING TECHNIQUES	72
<i>Krishnendu Chakrabarty</i>	
SECURITY DONE RIGHT: START AT THE HEART OF THE SOC.....	73
<i>Dana Neustadter</i>	
A NOVEL MINIMUM VARIANCE BEAMFORMER AND ITS CIRCUIT DESIGN FOR ULTRASOUND BEAMFORMING	74
<i>Ming Khuan Son, Neng-Jian Sim, Tzi-Dar Chiueh</i>	

VIDEO DEHAZING HARDWARE ACCELERATOR DESIGN BASED ON DARK CHANNEL PRIOR WITH SKY PRESERVATION	78
<i>Zi-Yi Zhao, An-Tai Xiao, Jiun-In Guo</i>	
HARDWARE ARCHITECTURE AND IMPLEMENTATION OF CLUSTERED TENSOR APPROXIMATION FOR MULTI-DIMENSIONAL VISUAL DATA	82
<i>Chi-Yun Yang, Yang-Ming Yeh, Yi-Chang Lu</i>	
FLEXIBLE MULTI-PRECISION ACCELERATOR DESIGN FOR DEEP CONVOLUTIONAL NEURAL NETWORKS CONSIDERING BOTH DATA COMPUTATION AND COMMUNICATION	85
<i>Shen-Fu Hsiao, Yu-Hong Chen</i>	
DESIGN OF A HIGH-THROUGHPUT AND AREA-EFFICIENT ULTRA-LONG FFT PROCESSOR	89
<i>Hong-Ke Lin, Pin-Han Lin, Chih-Wei Liu</i>	
RADIATION-HARDEN RISC PROCESSOR FOR MICRO-SATELLITES IN STANDARD CMOS.....	93
<i>Herming Chiueh, Chia-Hsiang Yang, Charles H.-P. Wen, Chao-Guang Yang, Po-Hao Chien, Ching-Yang Hung, Yu-Jui Chen, Yao-Pin Wang, Chin-Fong Chiu, Jer Lin</i>	
A 500NW-50 μ W INDOOR PHOTOVOLTAIC ENERGY HARVESTER WITH MULTI-MODE MPPT	95
<i>Ming-Chia Chang, Min-Hsuan Wu, Shen-Iuan Liu</i>	
AN SIMO STEP-DOWN CONVERTER WITH COUPLED INDUCTOR	99
<i>Yi-Chieh Hsu, Jing-Yuan Lin, Chii-Hwa Wang, Sz-Wei Chou</i>	
ANALYSIS AND DESIGN OF A SELF-CHARGED CRYSTAL OSCILLATOR WITH PULSE REGULATING FEEDBACK LOOP	103
<i>Hsiang-Chun Cheng, Yu-Hong Yang, Tai-Cheng Lee</i>	
A 1-200MHZ MULTIPLE OUTPUT FRACTIONAL DIVIDER USING PHASE ROTATING TECHNIQUE.....	107
<i>Chun-Yu Lin, Tun-Ju Wang, Yu-Ting Hung, Tsung-Hsien Lin</i>	
AN IMU-BASED WEARABLE RING FOR ON-SURFACE HANDWRITING RECOGNITION.....	109
<i>Zhe-Ting Liu, Davy P. Y. Wong, Pai H. Chou</i>	
INTEGRATED GROUP-BASED VALUABLE SENSOR SELECTION APPROACH FOR REMAINING MACHINERY LIFE ESTIMATION IN THE FUTURE INDUSTRY 4.0 ERA	113
<i>Kun-Chih Chen, Zi-Jie Gao</i>	
LOW-POWER 3D-PCB STACKING SYSTEM DESIGN AND VALIDATION BY AUTOMATIC VOLTAGE-CURRENT SCALABLE TECHNIQUE	117
<i>Ching-Hwa Cheng, Jiun-In Guo</i>	
A 24 MBIT/S RED LED-BASED VISIBLE LIGHT COMMUNICATION SYSTEM EMPLOYING DCO-OFDM MODULATION	119
<i>Yu-Jung Wang, Siou-Lin You, Zhen-Hao Zhu, Wei-Ting Lin, Cheng-You Ho, Chi-Lun Hsu, Chun-Hsing Lee, Hsi-Pin Ma</i>	
A MILLIMETER-WAVE FREQUENCY SYNTHESIZER FOR 60 GHZ WIRELESS INTERCONNECT	123
<i>Yong-Yu Lin, Fan-Ta Chen, Wei-Zen Chen</i>	

A 5.4GHZ $\Delta\Sigma$ BANG-BANG PLL WITH 19DB IN-BAND NOISE REDUCTION BY USING A NESTED PLL FILTER	125
<i>Xiaohua Huang, Bowen Wang, Woogeun Rhee, Zhihua Wang</i>	
A 0.5-V, 1.79- μ W, 250-KBPS WAKE-UP RECEIVER FOR IOT APPLICATION IN 90-NM CMOS.....	127
<i>Zhen-Cheng Zhang, Chun-Yuan Chiu, Hsiang-Cheng Yuan, Tsung-Hsien Lin</i>	
OVERVIEW OF THE OPENROAD DIGITAL DESIGN FLOW FROM RTL TO GDS.....	131
<i>Sherief Reda</i>	
PROGRAMMING SYSTEMS FOR PARALLELIZING VLSI CAD AND BEYOND.....	132
<i>Tsung-Wei Huang</i>	
BRINGING POWERFUL MACHINE-LEARNING SYSTEMS TO DAILY-LIFE DEVICES VIA ALGORITHM-HARDWARE CO-DESIGN	133
<i>Yingyan Lin</i>	
INTELLIGENT ARCHITECTURES FOR INTELLIGENT MACHINES	134
<i>Onur Mutlu</i>	
3D HETEROGENEOUS INTEGRATION TECHNOLOGY FOR AI SYSTEM	138
<i>Mitsumasa Koyanagi</i>	
EXCURSION PREVENTION STRATEGY TO INCREASE CHIP PERFORMANCE BY PHOTOMASK TUNING	139
<i>Ofir Sharoni, Yael Sufrin, Avi Cohen, Rolf Seltmann, Aravind Narayana, Thomas Thamm</i>	
MINIATURIZED CMOS IMAGING DEVICE FOR IMPLANTABLE APPLICATIONS.....	140
<i>Kiyotaka Sasagawa, Makito Haruta, Yasumi Ohta, Hironari Takehara, Jun Ohta</i>	
WEARABLES TO ELECTRONICS: THE KEY ENABLER FOR PERSONALIZED HEALTHCARE	141
<i>Jerald Yoo</i>	
BREATH ANALYSIS FOR EARLY DETECTION AND RAPID DIAGNOSIS OF DISEASES FOR PREVENTIVE MEDICINE	142
<i>Kea-Tiong Tang</i>	
EFFICIENT COMPUTING FOR AI AND ROBOTICS	143
<i>Vivienne Sze</i>	
MEMORY FOR DATA-CENTRIC COMPUTING: A TECHNOLOGY PERSPECTIVE	144
<i>Yih Wang</i>	
TAOX RERAM AS A HIGHLY-RELIABLE EMBEDDED MEMORY AND ITS APPLICATION TO EDGE AI.....	145
<i>Ryutaro Yasuhara</i>	
COMPUTE-IN-MEMORY FOR AI: FROM INFERENCE TO TRAINING.....	146
<i>Shimeng Yu</i>	
A COST-EFFECTIVE EMBEDDED NONVOLATILE MEMORY WITH SCALABLE LEE FLASH [®] -G2 SONOS FOR SECURE IOT AND COMPUTING-IN-MEMORY (CIM) APPLICATIONS.....	147
<i>Koji Nii, Yasuhiro Taniguchi, Kosuke Okuyama</i>	

5G EVOLUTION AND 6G..... 151
Takehiro Nakamura

Author Index