2020 IEEE International Test Conference India (ITC India 2020)

Bangalore, India 12-14 July 2020



IEEE Catalog Number: CFP20N34-POD ISBN: 978-1-7281-7459-4

Copyright © 2020 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP20N34-POD

 ISBN (Print-On-Demand):
 978-1-7281-7459-4

 ISBN (Online):
 978-1-7281-7458-7

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400

Fax: (845) 758-2633

E-mail: curran@proceedings.com Web: www.proceedings.com



ITC India 2020 Table of Contents

Table of Contents

Machine Learning Driven Throughput Optimization of Volume Diagnosis Methodology Sameer Chillarige, Anil Malik, Atul Chhabra, Bharath Nandakumar, Martin Amodeo, Nicholai L'Esperance, Robert Redburn, Jeff Zimmerman and Adisun Wheelock	1
Resource Optimal Realization of Fault-Tolerant Quantum Circuit	9
A non-ICL UVM approach to verifying DFx IJTAG network and its pros and conswersus the ICL-PDL approach	9
A Critical Engineering Dissection of LOS and LOC At-speed Test Approaches	4
Analyzing Fault Tolerance Behaviour in Memristor-based Crossbar for Neuromorphic Applications	1
Built-In Self-Repair for Manufacturing and Runtime TSV Defects in 3D ICs	0
Validating and Characterizing a 2.5D High Bandwidth Memory SubSystem 40 Sreeja Menon and Vinod Inipodu Murugan	6
An Efficient Hardware Trojan Detection Approach adopting Testability based Features 58 Priyadharshini Mohanraj and Saravanan P	5
Concealing Test Compression Mechanisms from Security Attacks	0
Machine Learning based Temperature Estimation for Test Scheduling of 3D ICs 6' Subhajit Chatterjee, Surajit Roy, Chandan Giri and Hafizur Rahaman	7
Fault Vulnerability Ranking of Transistors in Analog Integrated Circuits using AC Analysis	5
Wavelet transform based fault diagnosis in analog circuits with SVM classifier 83 Supriyo Srimani, Kasturi Ghosh and Hafizur Rahaman	3
A Hash based Secure Scheme (HSS) against scan-based attacks on AES cipher	3
Modeling and Test Generation for Combinational Hardware Trojans	7
Efficient Fault Detection and Diagnosis of Digital Microfluidic Biochip Using Multiple Electrodes Actuation	1