2020 IEEE 29th North Atlantic Test Workshop (NATW 2020)

Albany, New York, USA
17-24 June 2020

IEEE

IEEE Catalog Number: CFP20NAT-POD
ISBN: 978-1-7281-9700-5

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IEEE Catalog Number:	CFP20NAT-POD
ISBN (Print-On-Demand):	978-1-7281-9700-5
ISBN (Online):	978-1-7281-9699-2
ISSN:	2573-7589

Additional Copies of This Publication Are Available From:

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2020 IEEE North Atlantic Test Workshop *Virtual*
Papers Session
10AM to 12:35 - PM, Wednesday, June 17, 2020

The IEEE North Atlantic Test Workshop (NATW) provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 29th NATW features a general theme of "Achieving Semiconductor Reliability: Without Burn-In." The 2020 workshop is being held in 2 online sessions: June 17th papers session amd June 24th Tutorial/Panel.
Registration is a nominal fee which covers all sessions. Please register at "ieee.natw.org"
Zoom meetings will be used for the sessions. Once registered you will receive connection information.

NATW-2020 is sponsored by IEEE Schenectady Section and IEEE Region 1, and is supported by IBM Corp., Advantest America, AdamsIP, Mentor (A Siemens Business), Cadence Design Systems, Green Mountain Semiconductor and On Semiconductor.

Wednesday, June 17
10:00 am – 10:05 am Introduction and Welcome: Eugene Atwood General Chair
10:05 am – 10:10 am Introduction and Welcome: James Lloyd Program Chair
10:10 am – 10:40 am Invited Speaker: "Large-scale statistical analysis of early failures in Cu electromigration" Martin Gall With continuing scaling of Cu-based metallization, the electromigration failure risk has remained one of the most important reliability concerns for advanced process technologies. The main factors requiring attention are the activation energy related to the dominating diffusion mechanism, the current exponent as well as the median lifetimes and lognormal standard deviation values of experimentally acquired failure time distributions. In general, the origin and scaling behavior of these parameters are relatively well understood. However, the observation of bimodality in dual-inlaid Cu interconnects has added high complexity. Nanoscale electromigration-induced voids, requiring only a very limited amount of mass movement, can cause early failures and lead to severe concerns with respect to long-term, reliable chip operation at use conditions. For a more thorough investigation of these early failure phenomena, specific test structures were designed based on the Wheatstone Bridge technique. The use of these structures enabled an increase in the tested sample size past 800,000 for the 90 nm technology node, allowing a direct analysis of EM failure mechanisms at the single-digit ppm regime for the first time. These studies were continued for the 65, 40, 28, and 12 nm technologies, encompassing a total sample size of more than 1.5 million until the present time. This talk will give an overview of the development of the Wheatstone Bridge technique for early failure detection and highlight the main physical findings pertaining to the understanding of electromigration-induced degradation phenomena in advanced interconnects.

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	Martin Gall is the director of the Reliability Engineering Department at Globalfoundries in Malta, NY. He started his work in semiconductor reliability at Motorola/Freescale in 1995 as an engineer, He has (co)authored more than 70 publications, and is an editor for the IEEE Transactions on Device and Materials Reliability.
	Academic Contributions Format is 15 minutes and 5 minutes Q&A
1	**10:40 am – 11:00 am Paper 1: "A Built In Test circuit for waveform classification at high frequencies"** Konstantinos Poulos, Themistoklis Haniotakis We introduce a new Build In Test (BIT) signature generator for functional verification and output classification of RF integrated circuits. The proposed circuit is a single rectifier based MOS transistor, with the substrate and gate independently biased to control source terminal voltage range, followed by a passive RC filter. In normal operation the proposed low cost test scheme ensures the minimum effect at the performance of the measured circuit under test Presenting Author: Konstantinos Poulos, Southern Illinois University The author is currently a PhD student at Southern Illinois University in Carbondale at the Electrical and Computer engineering department. He is working in the field of VLSI and Test Automation. Recently returned from a 9-month internship as analog circuit designer. Currently my research involves DFT algorithms and BIT circuits
6	**11:00 am – 11:20 am Paper 2: "Calculating Signal Controllability using Neural Networks: Improvements to Testability Analysis and Test Point Insertion"** Joshua Immanuel and Spencer K. Millican This paper presents an artificial neural network-based signal probability predictor for VLSI circuits which considers reconvergent fan-outs. This study shows training and using artificial neural networks to predict signal probabilities increases post-test point insertion fault coverage compared to using COP, especially in circuits with many reconvergent fan-outs. Presenting Author: Spencer K. Millican Auburn University Dr. Millican is presently an Assistant Professor at Auburn University in Auburn, AL. He previously worked as a DFT engineer at the IBM Rochester Facility in Rochester, MN. He research interests include applying machine learning to DFT challenges and LBIST, and is the co-author numerous publications.

Industry Contributions 15 minutes and 5 minutes Q&A

12 **11:20 am – 11:40 am Paper 3: "Verification and Testing Considerations of an In-Memory AI Chip"** Marcia Golmohamadi, Ryan Jurasek, Wolfgang Hokenmaier, Don Labrecque, Ruoyo Zhi, Bret Dale,Nibir Islam, Dave Kinney, Angela Johnson

We present the testing and validation considerations for a programmable artificial neural network (ANN) integrated within a phase change memory (PCM) chip, featuring a Nor-Flash compatible serial peripheral interface (SPI). We introduce our method for validating the circuit components specific to the ANN application.

Presenting Author: Marcia Golmohamadi, Green Mountain Semiconductor
After finishing PhD's degree in Electrical Engineering at the University of Vermont in 2019, Marcia joined Green Mountain Semiconductor Inc. as a Circuit Design Engineer. Since then, she has been conducting research on development of a digital neuromorphic architecture to implement a programmable artificial neural network (ANN) inside a memory die. Author and/or Co-author of 13 papers and publications.

18 **11:40 am – 12:00 am Paper 4: "AI Powered THz VLSI Testing Technology"**
Naznin Akter, Mustafa Karabiyik, Michael Shur, John Suarez and Nezih Pala

We present a new terahertz testing technique for non-destructive identification of genuine integrated circuits, in package, in-situ and either with no or under bias, by measuring their response to scanning terahertz and sub-terahertz radiation at the circuit pins. By establishing and AI processing of the THz scanning signatures of reliable devices and circuits and comparing these signatures with devices under test using AI, this technology could be used for reliability and lifetime prediction

Presenting Author: Michael Shur, Electronics of the Future Patricia W. and C. Sheldon Roberts Professor at RPI and co-founder of Sensor Electronics Technology, Inc., and of Electronics of the Future, Inc. He is Fellow of IEEE, APS, ECS, OSA, and SPIE and Fellow of the National Academy of Inventors and of several other professional societies. He is an IEEE EDS Distinguished Lecturer and Foreign Member of the Lithuanian Academy of Sciences.

23 **12:00 am – 12:20 pm Paper 5: "Passive Intermodulation (PIM) Test and Measurement"**
Stephen Moss, Elanchezhian Veeramani and Joris Angelo Sundaram Jerome

PIM is a form of intermodulation distortion that occurs in passive components. It is an unwanted signal created by the mixing of two or more RF signals, caused by the nonlinearity of the passive components in the RF path. The paper describes the way PIM measurements are performed and highlights how Multiband PIM measurements are carried out in a very efficient way.

Presenting Author: Elanchezhian Veeramani, GlobalFoundries
Presently RF Characterization Engineer, GlobalFoundries, Essex Junction, Vermont. Previously with Exalt Wireless, Dallas, Texas. 6 years of experience in RF test methods, RF amplifiers and transceiver hardware debugging, calibrations, measurements with test equipment and technical analysis of point to point microwave radios used in backhaul networks.

26 **12:20 pm – 12:40 pm Paper 6: "Characterization of Thermal Runaway in a Ge Photodiode for Si Photonics"** Stewart Rauch, IEEE Life Fellow, Dongho Lee, Alexey Vert, and Roy Gupta

The power limits due to thermal runaway of a geranium PIN photo diode as the O-band (1300nm wavelength) photo detector component of a silicon photonics technology were characterized under elevated stress conditions. A simplified model is used to project to use condition.

Presenting Author: Stewart Rauch, GlobalFoundries
Principal Member of Technical Staff at GlobalFoundries, NY, working in the areas of reliability of Si photonics and RF CMOS. Formerly he was a faculty member at State University of New York, New Paltz and a Senior Technical Staff Member at IBM Semiconductor Research and Development Center (NY), specializing in hot carrier, bias temperature instability, and soft error reliability of state of the art CMOS technologies. He is a Life Fellow of IEEE

30 **12:40 pm – 1:00 pm Paper 7 "Self-heating characterization and its applications in technology development"** P. Paliwoda, M. Toledano-Luque, T. Nigam, F. Guarin, M. Nour, S. Cimino, L. Pantisano, A. Gupta, O. H. Gonzalez, M. Hauser, W. Liu, A. Vayshenker, D. Ioannou, D. Lee, L. Jiang, P. Yee, S. Rauch and B. Min

This work presents various device self-heating temperature sensing techniques and discusses their application in device reliability projection. Details of sensor design, technology choice, layout and ambient temperature impact on measurement results are discussed
Presenting Author: Peter Paliwoda, GlobalFoundries
Peter received the B.S. and M.S. degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2003 and 2005, respectively, and the Ph.D. degree in electrical and computer engineering from the New Jersey Institute of Technology in 2018. He is with GLOBALFOUNDRIES, Malta, NY, USA, researching front-end-of-line reliability with an emphasis on metal gate/high-k CMOS/RF technologies and thermal characterization/modeling

The seven papers above are to be published through IEEE