

2019 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH 2019)

**Qingdao, China
17 – 19 July 2019**



**IEEE Catalog Number: CFP19DTD-POD
ISBN: 978-1-7281-5521-0**

**Copyright © 2019 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP19DTD-POD
ISBN (Print-On-Demand):	978-1-7281-5521-0
ISBN (Online):	978-1-7281-5520-3
ISSN:	2327-8218

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Contents

<i>Design and Analysis of Majority Logic Based Approximate Radix-4 Booth Encoders</i>	1
Tingting Zhang, Weiqiang Liu, Jie Han and Fabrizio Lombardi	
<i>Graphene Nanoribbon-based Synapses with Versatile Plasticity.....</i>	7
He Wang, Nicoleta Cucu Laurenciu, Yande Jiang and Sorin Cotofana	
<i>Clifford Gate Optimisation and T Gate Scheduling: Using Queueing Models for Topological Assemblies.....</i>	13
Alexandru Paler and Robert Basmadjian	
<i>Novel 3D architecture of the ISIR devices</i>	18
Behnoush Attarimashalkoubeh and Yusuf Leblebici	
<i>ComPRIME: A Compiler for Parallel and Scalable ReRAM-based In-Memory Computing...</i>	20
Steffen Frerix, Saeideh Shirinzadeh, Saman Fröhlich and Rolf Drechsler	
<i>ESL: A Robust Memristor-based Logic Design Resilient to Resistance Variation.....</i>	26
Jintao Yu, Hoang Anh Du Nguyen, Muath Abu Lebdeh, Mottaqiallah Taouil and Said Hamdioui	
<i>Experimental Investigation of Memristance Enhancement</i>	32
Vasileios Ntinias, Antonio Rubio, Georgios Ch. Sirakoulis, Rosana Rodríguez and Montserrat Nafria	
<i>A Self-Timing Voltage-Mode Sense Amplifier for STT-MRAM Sensing Yield Improvement. </i>	34
Yongliang Zhou, Menglin Han, Mingyue Liu, Hao Cai, Jun Yang and Bo Liu	
<i>A Novel Memristor-Reusable Mapping Methodology of In-memory Logic Implementation for High Area-Efficiency</i>	40
Yongjie Lu, Yanan Sun, Weifeng He and Zhigang Mao	
<i>Process Variation-Resilient STT-MTJ based TRNG using Linear Correcting Codes.....</i>	46
Rashid Ali, You Wang, Zhengyi Hou, Haoyuan Ma, Youguang Zhang and Weisheng Zhao	
<i>Spintronic Memories: From Memory to Computing-in-Memory</i>	52
Wang Kang, He Zhang and Weisheng Zhao	
<i>REAL: Logic and Arithmetic Operations Embedded in RRAM for General-Purpose Computing</i>	54
Lei Xie, Hao Cai and Jun Yang	
<i>Dynamic Adaptation of Approximate Bit-width for CNNs based on Quantitative Error Resilience</i>	58
Chengjun Wu, Weiwei Shan and Jiaming Xu	
<i>Detecting and Bypassing Trivial Computations in Convolutional Neural Networks</i>	64
Dongning Ma and Xun Jiao	
<i>An Energy-Efficient Architecture for Accelerating Inference of Memory-Augmented Neural Networks</i>	70
Jianxun Yang, Leibo Liu, Shaojun Wei, Shouyi Yin and Jin Zhang	

<i>Implementing Binarized Neural Networks with Magnetoresistive RAM without Error Correction</i>	76
Tifenn Hirtzlin, Bogdan Penkovskiy, Jacques-Olivier Klein, Nicolas Locatelli, Adrien F. Vincent, Marc Bocquet, Jean-Michel Portal and Damien Querlioz	
<i>An Energy-Efficient In-Memory BNN Architecture With Time-Domain Analog and Digital Mixed-Signal Processing</i>	81
Tao Wang and Weiwei Shan	
<i>Ring-Shaped Content Addressable Memory Based On Spin Orbit Torque Driven Chiral Domain Wall Motions</i>	87
Yue Zhang, Jiang Nan, Guanda Wang, Xueying Zhang, Youguang Zhang and Weisheng Zhao	
<i>ResNet Can Be Pruned 60x: Introducing Network Purification and Unused Path Removal (P-RM) after Weight Pruning</i>	89
Xiaolong Ma, Geng Yuan, Sheng Lin, Zhengang Li, Hao Sun and Yanzhi Wang	
<i>A Logic Simplification Approach for Very Large Scale Crosstalk Circuit Designs</i>	91
Md Arif Iqbal, Naveen Kumar Macha, Bhavana Tejaswini Repalle and Mostafizur Rahman	
<i>Effect of Lattice Defects on the Transport Properties of Graphene Nanoribbon</i>	97
Konstantinos Rallis, Panagiotis Dimitrakis, Georgios Ch. Sirakoulis, Ioannis Karafyllidis and Antonio Rubio	
<i>Plasma Modified Silicon Nitride Resistive Switching Memories</i>	99
Panagiotis Dimitrakis, Panagiotis Karakolis, Pascal Normand, Georgios Ch. Sirakoulis and Ioannis Karafyllidis	
<i>High speed and reliable Sensing Scheme with Three Voltages for STT-MRAM</i>	101
Jinkai Wang, Yue Zhang, Chenyu Lian, Guanda Wang, Kun Zhang, Xiulong Wu, Youguang Zhang and Weisheng Zhao	
<i>A compact model of stochastic switching in STT magnetic RAM for memory and computing</i>	107
Roberto Carboni, Elena Vernocchi, Manzar Siddik, Jon Harms, Andy Lyle, Gurtej Sandhu and Daniele Ielmini	
<i>Comprehensive Pulse Shape Induced Failure Analysis in Voltage-Controlled MRAM.....</i>	113
Mingyue Liu, Menglin Han, Lei Xie, Jun Yang, Lirida Naviner and Hao Cai	
<i>Low-Power, High-Speed and High-Density Magnetic Non-Volatile SRAM Design with Voltage-Gated Spin-Orbit Torque.....</i>	119
Chengzhi Wang, Deming Zhang, Lang Zeng, Kaili Zhang, Youguang Zhang and Weisheng Zhao	
<i>Thermal Stable and Fast Perpendicular Shape Anisotropy Magnetic Tunnel Junction.....</i>	125
Guanda Wang, Yue Zhang, Zhe Huang, Jinkai Wang, Kun Zhang, Zhizhong Zhang, Youguang Zhang and Weisheng Zhao	
<i>Enabling New Computing Paradigms with Emerging Symmetric-Access Memories.....</i>	131
Juejian Wu, Mingyang Gu, Hongtao Zhong, Yunsong Tao, Fei Qiao, Huazhong Yang and Xueqing Li	
<i>Deep Neural Network Acceleration in Non-Volatile Memory: A Digital Approach.....</i>	137
Shaahin Angizi and Deliang Fan	
<i>Non-volatile Logic and Memory based on Reconfigurable Ferroelectric Transistors.....</i>	143
Sandeep Krishna Thirumala, Arnab Raha, Vijaykrishnan Narayanan, Vijay Raghunathan and Sumeet Gupta	

Technology-Assisted Computing-In-Memory Design for Matrix Multiplication Workloads 149

Nicholas Jao, Srivatsa Srivinasu, Akshay Krishna Ramanathan, Minhwan Kim, John Sampson and
Vijaykrishnan Narayanan

List of Authors 155