

2020 Argentine Conference on Electronics (CAE 2020)

**Buenos Aires, Argentina
27 – 28 February 2020**



**IEEE Catalog Number: CFP20S41-POD
ISBN: 978-1-7281-6196-9**

**Copyright © 2020 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP20S41-POD
ISBN (Print-On-Demand):	978-1-7281-6196-9
ISBN (Online):	978-1-7281-6195-2

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Table of Contents

An annotated guide to utilize ring-oscillators as thermal sensor in FPGA technology	1
<i>Luciana De Micco, Carlos Minchola, John Leon-Franco, Eduardo Boemo and Maximiliano Antonelli</i>	
SiPM Analog Front-End Electronics For Space-Borne Applications INVITED PAPER	8
<i>Nahuel Muller, Federico Izraelevitch, Pablo Levy, Matías Cveczilbeg, Gabriel Sanca and Federico Golmar</i>	
High-Speed Data Acquisition System for GNSS Applications	14
<i>Jorge G. Vega Leañez, José I. Barbería, Santiago Rodríguez, Juan G. Díaz, Ramón López La Valle, Javier G. Garcia and Carlos Muravchik</i>	
Sensitive Devices and Phase Noise Degradation Mechanisms on all-NMOSFET RF VCO Aging . . .	20
<i>Sebastian Matías Pazos, Juan José Baudino, Matías Nicolás Joglar, Fernando Leonel Aguirre, Carlos Navarro, Felix Palumbo and Fernando Silveira</i>	
Device Mismatching and Random Telegraph Signal In Digital Pixel Imagers On 90-nm CMOS Process	27
<i>Charbel Rizk, Alejandro Pasciaroni, Pedro Julian, H. Radhakrishnan, J. Wilson and Philippe Pouliquen</i>	
MOS Devices and Integrated Circuits for Ionizing Radiation Dosimetry: a Review	31
<i>Mariano Garcia-Inza, Sebastián Carbonetto and Adrian Faigon</i>	
Successive Interference Cancellation for the NB-IoT Uplink Multiple Access	41
<i>Gustavo J. González, Fernando Gregorio and Juan Cousseau</i>	
A Variable Gain and Bandwidth Fully Differential CMOS Neural Preamplifier	47
<i>Luciano Martinez Rau</i>	
A simple BLOCK interleaving algorithm using reduced memory and address generator resources . .	53
<i>Guillermo Jaquenod and Gerado Acosta</i>	
Implementation of a Polyphase Filter Bank Channelizer on a Zynq FPGA	57
<i>Luis Horacio Arnaldi</i>	
Design of a Rectenna for Energy Harvesting on Wi-Fi at 2.45 GHz	63
<i>Andry Contreras, Benigno Rodríguez, Leonardo Steinfeld, Javier Schandy and Mariana Siniscalchi</i>	
X-ray spectroscopy up to 17.6 keV using a Commercial Off The Shelf CMOS Image Sensor	69
<i>Martín Pérez, Miguel Sofo Haro, Juan Jerónimo Blostein, Andres Cicutin, Maria Liz Crespo, Fabricio Alcalde Bessia, Ivan Sidelnik, Mariano Gómez Berisso and José Lipovetzky</i>	
Characterization of a low-power CMOS operational amplifier from 12.5K to 273K for low temperature experiments	73
<i>Jose Lipovetzky, Fabricio Alcalde Bessia, Julio Guimpel, Martín Pérez and Mariano Gómez Berisso</i>	

A 4GS/s 8-bit SAR ADC with an Energy-Efficient Time-Interleaved Architecture in 130nm CMOS	77
<i>Benjamin T. Reyes, Laura Biolato, Agustin C. Galetto, Leandro Passetti, Fredy Solis, Juan I. Giubilatto, Leandro A. Reyes, Alvaro Fernandez Bocco and Mario R. Hueda</i>	
A Self-biased Current Source, using an Asymmetric Bulk-modified MOS Composite Transistor	82
<i>Diego Costa, Matías Miguez, Joel Gak, Fabián Torres and Alfredo Arnaud</i>	
The new data acquisition system of the LAGO Collaboration based on the Redpitaya board	87
<i>Luis Horacio Arnaldi, Ivan Sidelnik, Dennis Cazar and Mario Audelo</i>	
An Integrated 350V Dimmer	93
<i>Fabian Torres Alvarez, Joel Gak, Alfredo Arnaud and Matias Miguez</i>	
System-on-Chip Implementation of a Self-Configuration System for a Programmable Photodetector ASIC	99
<i>Lucas Mombello, Nicolás Calarco and Fernando Perez Quintián</i>	
Design of ESD Protections for ECG Applications	104
<i>Pablo Gardella, Eduardo Baez and Juan Cesaretti</i>	
Simplicial Piecewise Linear Computation Complexity for Vector-Vector Products	108
<i>Pedro Julian and Martin Villemur</i>	