

# **2019 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS 2019)**

**Portland, Oregon, USA  
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**Wednesday, September 25, 2019**

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**10:50 Session I: PTP and NTP Security**

**Belmont A**

**Session Chair:** Kang B Lee (NIST, USA)

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**Next Steps in Security for Time Synchronization: Experiences from implementing IEEE 1588 v2.1** %

*Ezzeldin Shereen (KTH Royal Institute of Technology, Sweden)*

*Florian Bitard (KTH Royal Institute of Technology & French Civil Aviation University, France)*

*György Dán (KTH Royal Institute of Technology, Sweden)*

*Tolga Sel (Siemens AG, Germany)*

*Steffen Fries (Siemens AG, Germany)*

**Secure Precision Time Protocol in Packet Switched Networks** +

*Prasanth Kemparaj (Juniper Networks, India)*

*Satheesh Kumar S (Juniper Networks, India)*

**Guards and Watchdogs in One-Way Synchronization with Delay-Related Authentication Mechanisms** %

*Martin Langer (Ostfalia Hochschule Wolfenbüttel, Germany)*

*Kristof Teichel (Physikalisch-Technische Bundesanstalt, Germany)*

*Kai Heine (Ostfalia Hochschule Wolfenbüttel, Germany)*

*Dieter Sibold (Physikalisch-Technische Bundesanstalt, Germany)*

*Rainer Bermbach (Ostfalia Hochschule Wolfenbüttel, Germany)*

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**13:15 Session I: PTP and NTP Security (continued)**

**Belmont A**

**Session Chair:** Kang B Lee (NIST, USA)

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**Redundant Schemes or How to Counter the Delay Attack on Time Synchronization Protocols** %

*Cristian Marinescu (OMICRON Electronics GmbH, Austria)*

*Johannes Neyer (OMICRON, Austria)*

*Lukas Gassner (OMICRON, Austria)*

**Securing Unprotected NTP Implementations Using an NTS Daemon** &

*Martin Langer (Ostfalia Hochschule Wolfenbüttel, Germany)*

*Thomas Behn (Meinberg Funkuhren GmbH & Co. KG, Germany)*

*Rainer Bermbach (Ostfalia Hochschule Wolfenbüttel, Germany)*

Thursday, September 26, 2019

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10:30 **Session II: Measurements, Monitoring, and Calibration**

**Belmont A**

**Session Chair:** Douglas Arnold (Meinberg, USA)

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**In situ determination of the fiber delay coefficient in time-dissemination networks** %

*Peter Jansweijer (Nikhef, The Netherlands)*

*Henk Peek (Nikhef, The Netherlands)*

**Exploiting Smartphone Peripherals for Precise Time Synchronization** +

*Sandeep Sandha (UCLA, USA)*

*Joseph Noor (University of California, Los Angeles, USA)*

*Fatima M Anwar (University of California Los Angeles, USA)*

*Mani B. Srivastava (University of California, Los Angeles, USA)*

**ARTT: A Scalable Approach for Monitoring the Quality of Time in Distributed Systems** ' .

*Brandon Smith (University of New Hampshire & University of New Hampshire Interoperability Laboratory, USA)*

*Robert Noseworthy (University of New Hampshire, USA)*

*Radim Bartos (University of New Hampshire, USA)*

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13:15 **Session II: Measurements, Monitoring, and Calibration (continued)**

**Belmont A**

**Session Chair:** Douglas Arnold (Meinberg, USA)

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**Calibrating NTP** -

*Faten Mkacher (Grenoble Informatics Laboratory & Gorgy Timing Company, France)*

*Andrzej Duda (Grenoble Institute of Technology, France)*

**Test Results of IEEE 1588v2 Network Synchronization Holdover Performance using Various Types of Reference Oscillators** )

*Robert M Kaminsky (Silicon Labs, USA)*

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**14:05 Session III: Power, Industrial, and IoT Applications**

**Belmont A**

**Session Chair:** Radim Bartos (University of New Hampshire, USA)

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**Are Cloud Services Aware of Time? An Experimental Analysis oriented to Industry 4.0\*\*\*\*\* \$**

*Stefano Rinaldi (University of Brescia, Italy)*

*Paolo Bellagente (University of Brescia, Italy)*

*Paolo Ferrari (University of Brescia, Italy)*

*Alessandra Flammini (University of Brescia, Italy)*

*Emiliano Sisinni (University of Brescia, Italy)*

**A timing impairment module for electrical synchro metrology\*\*\*\*\* \***

*Dhananjay Anand (NIST, USA)*

*Colin Freiheit (University of Vermont, USA)*

*Marc Weiss (Marc Weiss Consulting & NIST, USA)*

*Kishan Shenoi (Qulsar, USA)*

*Hamid Ossareh (University of Vermont, USA)*

**Software-based Time Synchronization for Integrating Power Hardware in the Loop Emulation in IEEE1588 Power Profile Testbed\*\*\*\*\*+'**

*Stefano Rinaldi (University of Brescia, Italy)*

*Federico Bonafini (University of Brescia, Italy)*

*Paolo Ferrari (University of Brescia, Italy)*

*Alessandra Flammini (University of Brescia, Italy)*

*Marco Pasetti (University of Brescia, Italy)*

*Emiliano Sisinni (University of Brescia, Italy)*