

# **2019 41st Annual EOS/ESD Symposium (EOS/ESD 2019)**

**Riverside, California, USA  
15 – 20 September 2019**



**IEEE Catalog Number: CFP19413-POD  
ISBN: 978-1-7281-2890-0**

**Copyright © 2019, Electrical Overstress/Electrostatic Discharge Association, Inc.  
All Rights Reserved**

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP19413-POD
ISBN (Print-On-Demand):	978-1-7281-2890-0
ISBN (Online):	978-1-58537-311-6
ISSN:	0739-5159

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# TABLE OF CONTENTS

## 1A: Advanced CMOS EOS/ESD and Latch-up

Moderator: Souvick Mitra, GlobalFoundries

<a href="#"><u>1A.1 Transient Overshoot of Sub-10 nm Bulk FinFET ESD Diodes with S/D Epitaxy Stressor</u></a>	1
Shih-Hung Chen, Dimitri Linten, Geert Hellings, Marko Simicic, Thomas Chiarella, Pierre Eyben, Stefan Kubicek, Erik Rosseel, Andriy Hikavyy, Anda Mocuta, Naoto Horiguchi, imec	
<a href="#"><u>1A.2 Low-Capacitance SCR for On-Chip ESD Protection with High CDM Tolerance in 7nm Bulk FinFET Technology</u></a>	9
Po-Lin Peng, Li-Wei Chu, Ming-Fu Tsai, Yu-Ti Su, Jam-Wem Lee, Kuo-Ji Chen, Ming-Hsiang Song, Taiwan Semiconductor Manufacturing Company	
<a href="#"><u>1A.3 External Latch-up Risks and Prevention Solutions in Advanced Bulk FinFET Technology</u></a>	14
Wei Liang, Robert Gauthier Jr., Souvick Mitra, Hien Lai, GLOBALFOUNDRIES	
<a href="#"><u>1A.4 ESD Protection Diode with Guard Ring Layout Optimized for Latch-up Immunity Enhancement in FinFET Technology</u></a>	23
Kai-Ping Huang, Po-Lin Peng, Li-Wei Chu, Yi-Feng Chang, Tzu-Heng Chang, Jam-Wem Lee, Kuo-Ji Chen, Ming-Hsiang Song, Taiwan Semiconductor Manufacturing Company	
<a href="#"><u>1A.5 Low-Leakage NMOS Clamps with Gate-Assisted Bipolar Triggering</u></a>	27
Michael Stockinger, NXP Semiconductors	

## 1B: Manufacturing I

Moderator: Rita Fung, Cisco

<a href="#"><u>1B.1 Design of a Critical Application Air Ionizer for Semiconductor Manufacturing</u></a>	37
Larry Levit, LBL Scientific; Gregory Larson, Alan Mccall, Julian Montoya, Intel Corporation; Timothy Maroni, NRD LLC; Geoffrey Weil, Anodyne Research; Jeremy Willden, Constellation Labs LLC	
<a href="#"><u>1B.2 CPM Test Limitation Study for AC, Pulsed AC and High Frequency AC Ionizers vs. DC Based Ionizers</u></a>	44
Joshua (YongHoon) Yoo, Ethan (YoungChul) Choi, Elly (SoYoung) Koo, Core Insight, Inc.	
<a href="#"><u>1B.3 A Low-Voltage Microwave Plasma Ionizer Without the ESD Risk Due to a High Voltage Source</u></a>	53
Byoungjin Bae, Jinghool Kim, Ulsan National Institute of Science and Technology	
<a href="#"><u>1B.4 Characterization of ESD Shielding Bag with Capacitive Probe and IEC 61000-4-2 Generator</u></a>	60
Toni Viheriakosko, Cascade Metrology; Rita Fund, Richard Wong, Cisco Systems; Reinhold Gaertner, Friedrich zur Nieden, Infineon Technologies AG; Pasi Tamminen EDR & Medeso Oy	
<a href="#"><u>1B.5 Evaluation of ESD Garment with Conductive Ribbon</u></a>	70
Bernard Chin, Jeremy Ong, UTAC Headquarters Pte Ltd.; L.H. Koh, Everfeed Technology Pte. Ltd.	

## **2A: EOS/ESD Failure Analysis, Troubleshooting, and Case Studies 1**

Moderator: Ann Concannon, Texas Instruments

**2A.1 HV Latch-up at System Level ESD Current Injection** 74  
David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp.

**2A.2 Mechanism of Sequential Finger Triggering of Multi-Finger Floating-Base SCR's Due to Inherent Substrate Currents** 81  
Hasan Karaca, Clement Fleury, Dionyz Pogany, TU Wien; Steffen Holland, Hans-Martin Ritter, Guido Notermans, Nexperia Germany GmbH

**2A.3 Dual Injection Latch-up Phenomenon in HV Rail Based ESD Protection Networks** 91  
Slavica Malobabic, David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp

## **2B: Full-Custom and Application Drive ESD Concepts**

Moderator: Christian Russ, Infineon Technology

**2B.1 Phase Change Disabling Circuit for the Poly Fuse During the ESD Event** 99  
Shao-Chang Huang, Li-Fan Chen, Chun-Chih Chen, Ting-You Lin, Kai-Chieh Hsu, Yeh-Ning Jou, Chih-Hsuan Lin, Yung Chang Chen, Wei-Sung Chen, Jian Hsing Lee, Vanguard International Semiconductor Corporation

**2B.2 Concurrent ESD and Surge Protection Clamps in RF Power Amplifier** 109  
Myunghwan Park, Jermyn Tseng, Tzung-yin Lee, David Ripley, Skyworks Solutions, Inc.

**2B.3 A 3-Terminal HV-ESD Protection as Specialized Solution for EDn-MOSTs that Directly Link Two External Pads** 115  
Gijs de Raad, Da-Wei Lai, NXP Semiconductors

## **3A: EOS/ESD Failure Analysis, Troubleshooting, and Case Studies 2**

Moderator: Shih-Hung Chen, imec

**3A.1 3.3V ESD Clamp Structure Susceptibility Towards Pseudo LU in 22FDSOI** 125  
Anurag Mittal, Nitin Bansal, Invecas Technologies Pvt., Ltd.

**3A.2 ESD Design Considerations for Ultra-Low Power Crystal Oscillators in Automotive Products** 130  
Stefan Dannenberger, Oddgeir Fikstvedt, Danielle Griffith, Texas Instruments

**3A.3 EOS Protection of the Low Voltage Gate Oxide Devices** 136  
Vladislav Vashchenko, Slavica Malobabic, Maxim Integrated Corp.

## **3B: Manufacturing II**

Moderator: Michelle Lam, IBM

### **3B.1 WITHDRAWN**

**3B.2 Circular Aperture Effects on Radiated Emissions of Electrostatic Discharge Events** 142  
Gregory Larson, Intel Corporation

<b><u>3B.3 Measurement of Electrostatic Discharge Through Human Bodies Contacting Metallic Objects Under HVAC Transmission Lines</u></b>	149
Tiebing Lu, North China Electric Power University; Xiuying Li, Norendar International Ltd.	
<b><u>3B.4 Poster – Ionized Electric Field due to HVDC Corona Discharge</u></b>	N/A
Tiebing Lu, North China Electric Power University	
<b>4A: System Level EOS/ESD/EMC 1</b>	
Moderator: Robert Ashton, Minotaur Labs	
<b><u>4A.1 A Variable <math>V_h</math> Combined Power Clamp for System Level ESD/ Surge Immunity Enhancement with Low Leakage</u></b>	155
Koki Narita, Mototsugu Okushima, Renesas Electronics Corporation	
<b><u>4A.2 Saturation Attenuator for TVS Devices</u></b>	161
Eugene R. Worley, Silicon Crossing LLC	
<b><u>4A.3 Development of EMC Analysis Technology Using Large-Scale Electromagnetic Field Analysis</u></b>	171
Ryo Matsubara, Katsuo Inokuchi, Panasonic Corporation	
<b><u>4A.4 HMM Failure Level Variations Revisited</u></b>	177
Marcel Dekker, MASER Engineering; Theo Smedes, NXP Semiconductors; Guido Notermans, Nexperia Germany GmbH, Robert Ashton, Minotaur Labs	
<b><u>4A.5 ESD<sub>21</sub>, an Approach to Characterize Behavior of Multiport ICs Under ESD Stress</u></b>	185
Omid Hoseini Izadi, David Pommerenke, Missouri University of Science and Technology; Kathy Muhonen, Nate Peachey, Qorvo, Inc.	
<b>4B: Manufacturing 3</b>	
Moderator: Dale Parkin, Seagate Technology	
<b><u>4B.1 Captive Discharge to Ground of a Flat Metal Disk with a Pin Contact</u></b>	193
Icko Eric Timothy Iben, IBM Co.	
<b><u>4B.2 Discharge Current Analysis with Charged Connector Pins</u></b>	203
Pasi Tamminen EDR@Medeso; Rita Fung, Rick Wong, Cisco Systems, Inc.	
<b><u>4B.3 Are ESD Chairs Good Enough to be Used as Primary Means of Personnel Grounding</u></b>	212
Reinhold Gartner, Magdalena Hikersberger, Infineon Technologies AG; Wolfgang Stadler, Josef Niemesheim, Intel Deutschland GmbH; Jurgen Speicher, Wolfgang Warmbier GmbH & Co. KG	
<b><u>4B.4 Determining the Proper Methods of Measuring a Conveyor Belt’s Resistance to Ground</u></b>	222
Donn G. Bellmore, Advanced ESD Services +; Richard Strube, Universal Instruments Corporation	
<b><u>4B.5 Dummy Versus Live ESD Sensitive Devices Charge Analysis for Automated Handling Equipment ESD Qualification</u></b>	228
Jeremy Ong, Bernard Chin, UTAC Headquarters Pte Ltd.; L.H.Koh Everfeed Technology Pte. Ltd.	

## 5A: System Level ESD 2

Moderator: Guido Notermans, Nexperia

### [5A.1 Application Example of a Novel Methodology to Generate IC Models for System ESD and Electrical Stress Simulation out of the Design Data](#) 233

Michael Ammer, Infineon Technologies AG, University of the Federal Armed Forces Munich; Andreas Rupp, Yiqun Cao, Infineon Technologies Ag; Martin Sauter, Linus Maurer University of the Federal Armed Forces Munich

### [5A.2 TVS Devices Transient Behavior Modeling Framework and Application to SEED](#) 241

Li Shen, Shubhankar Marathe, Javad Meiguni, Guangxiao Luo, Jianchi Zhou, David Pommerenke, Missouri University of Science and Technology

### [5A.3 Characterizing and Modeling Common Mode Inductors at High Current Levels for System ESD Simulations](#) 251

Michael Ammer, Infineon Technologies AG, University of the Federal Armed Forces Munich; Andreas Rupp, Infineon Technologies AG; Martin Sauter, Linus Maurer, University of the Federal Armed Forces Munich

## 6A: Numerical Modeling and Electronic Design Automation 1

Moderator: Nitesh Trivedi, Intel

### [6A.1 Impact of Lowly Doped Regions on Transient Overshoot Voltage During vf-TLP Pulses for Bipolar Devices](#) 258

Steffen Holland, Guido Notermans, Hans-Martin Ritter, Nexperia Germany GmbH

### [6A.2 ESD Protection Impact and Modelling of Bias-Dependent Series Resistance in Diodes](#) 264

Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar, Analog Devices, Inc.

### [6A.3 A Comprehensive Physical Model for PNP Based ESD Protection Devices in SOI Technology](#) 271

Xiaoliang Han, Shuang Zhao, NXP Semiconductors

## 7A: Modeling 2

Moderator: Nitesh Trivedi, Intel

### [7A.1 Towards a TCAD Model for NMOS Loads in 28FD-SOI Under TLP & \(vf\)-TLP Transient Condition](#) 278

Gabriel-Dumitru Cretu, Filippo Magrini, Friedrich zur Nieden, Kai Esmark, Infineon Technologies

### [7A.2 Simulation Driven ESD Current Density Check](#) 284

Ulrich Glaser, Radu Stoica, Radu Ionescu, Marcel Preda, Infineon Technologies

## **8A: Testing**

Moderator: Theo Smedes, NXP

### **8A.1 Towards Standardization of Low Impedance Contact CDM** 290

Nathan Jack, Brett Carn, Josh Morris, Intel Corporation

### **8A.2 Study of CDM Measurement for Bare Die and Wafers** 297

Teruo Suzuki, Kazuya Okubo, Hiroki Taniguchi, Socionext, Inc; Masanori Sawada, Hiroyuki Okumura, Kazuo Shinke, Hanwa Electronic Ind. Co; Osamu Mihama, Mihama Corp.

### **8A.3 Energy of CDM Failure of ICs on Package-, Wafer-, and Board-Level** 304

Lena Zeithoefler, Friedrich zur Nieden, Kai Esmark, Gernot Langguth, Infineon Technologies AG

### **8A.4 Low Impedance Contact CDM – Evaluation and Modeling** 314

Marko Simicic, Wei-Min Wu, Shih-Hung Chen, Dimitri Linten, imec; Nathan Jack, Intel Corp.; Shinichi Tamura, Yohei Shimada, Masanori Sawada, Hanwa Electric Ind. Co., Ltd.

# Workshops

Workshops Chair – Souvick Mitra, GLOBALFOUNDRIES, Inc, Essex Junction, VT

## Workshop Session A

**A.1: Sub-150V CDM Testing** 323  
*Moderators: Nathan Jack, Intel Corporation; Alan Righter, Analog Devices*

**A.2: Machine Learning and More: Advancement in Simulation and EDA Methods for ESD Verification** 324  
*Moderators: Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Norman Chang, ANSYS; Robert Gauthier, GlobalFoundries; Michael Khazhinsky, Silicon Labs*

**A.3: 3<sup>rd</sup> Party IP and Foundry Deliveries – Problem Solved for Seamless, ESD Safe IC Top Level Integration** 325  
*Moderators: Harald Gossner, Intel Deutschland GmbH*

**A.4: EOS Best Practices** 326  
*Moderators: Vladimir Kraz, On Filter, Inc.*

## Workshop Session B

**B.1: Adapting to the Demands of Automotive – From an ESD Perspective** 327  
*Moderators: Ann Concannon, Texas Instruments, Inc.*

**B.2: IEC Testing** 328  
*Moderators: Nate Peachey, Qorvo Inc.; Andrew Spray, David Klein, Synpatics, Inc.*

**B.3: ESD Myths and Misconceptions** 329  
*Moderators: Dana Beatty, Xfabion; Matt Jane, Tesla; Andy Nold, Eagle Test Systems, a Teradyne Company*

**B.4 IoT devices for consumer, automated and industrial – Where is special need for IP, EDA tools and technology to support ESD and reliability?** 330  
*Moderator: Harald Gossner, Intel Deutschland GmbH*

## Biographies

## Past Awards and Presentations