

**2019 IEEE/ACM 7th
International Conference on
Formal Methods in Software
Engineering (FormaliSE 2019)**

**Montreal, Quebec, Canada
27 May 2019**



**IEEE Catalog Number: CFP19ZAP-POD
ISBN: 978-1-7281-3374-4**

**Copyright © 2019 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP19ZAP-POD
ISBN (Print-On-Demand):	978-1-7281-3374-4
ISBN (Online):	978-1-7281-3373-7
ISSN:	2380-873X

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2019 IEEE/ACM 7th International Conference on Formal Methods in Software Engineering (FormaliSE) **FormaliSE 2019**

Table of Contents

Message from ICSE 2019 General Chair	vii
Message from the Chairs of FormaliSE 2019	ix
Program Committee	x
Subreviewers	xi

FormaliSE 2019 - Session 1

Epistemic Model Checking of Distributed Commit Protocols with Byzantine Faults	1
<i>Omar Al-Bataineh (Nanyang Technological University) and Mark Reynolds (University of Western Australia)</i>	
Rigorous Design and Deployment of IoT Applications	11
<i>Ajay Krishna (Univ. Grenoble Alpes, Inria, CNRS), Michel Le Pallec (Nokia Bell Labs), Radu Mateescu (Univ. Grenoble Alpes, Inria, CNRS), Ludovic Noirie (Nokia Bell Labs), and Gwen Salaün (Univ. Grenoble Alpes, CNRS)</i>	
Static Analysis for Worst-Case Battery Utilization	21
<i>Dmitry Ivanov (Hamburg University of Technology) and Sibylle Schupp (Hamburg University of Technology)</i>	
Clock Reduction in Timed Automata While Preserving Design Parameters	31
<i>Beyazit Yalcinkaya (Middle East Technical University) and Ebru Aydin Gol (Middle East Technical University)</i>	

FormaliSE 2019 - Session 2

FASTEN: An Open Extensible Framework to Experiment with Formal Specification Approaches	41
<i>Daniel Ratiu (Siemens Corporate Technology, Germany), Marco Gario (Siemens Corporate Technology, USA), and Hannes Schoenhaar (Siemens Corporate Technology, Germany)</i>	

FormaliSE 2019 - Session 3

Parallelizable Reachability Analysis Algorithms for Feed-Forward Neural Networks .51.....	51
<i>Hoang-Dung Tran (Vanderbilt University), Patrick Musau (Vanderbilt University), Diego Manzananas Lopez (Vanderbilt University), Xiaodong Yang (Vanderbilt University), Luan Viet Nguyen (University of Pennsylvania), Weiming Xiang (Vanderbilt University), and Taylor T Johnson (Vanderbilt University)</i>	
Towards Sampling and Simulation-Based Analysis of Featured Weighted Automata .61.....	61
<i>Maxime Cordy (SnT, University of Luxembourg), Axel Legay (Université Catholique de Louvain), Sami Lazreg (Université Côte d'Azur), and Philippe Collet (Université Côte d'Azur, CNRS)</i>	
Verifying Channel Communication Correctness for a Multi-core Cooperatively Scheduled Runtime Using CSP .65.....	65
<i>Jan Bækgaard Pedersen (University of Nevada Las Vegas) and Kevin Chalmers (Edinburgh Napier University)</i>	
A Generalized Program Verification Workflow Based on Loop Elimination and SA Form .75.....	75
<i>Cláudio Belo Lourenço (LRI, Université Paris-Sud & INRIA Saclay), Maria João Frade (HASLab/INESC TEC & Universidade do Minho), and Jorge Sousa Pinto (HASLab/INESC TEC & Universidade do Minho)</i>	

FormaliSE 2019 - Session 4

Modular Synthesis of Verified Verifiers of Computation with STV Algorithms .85.....	85
<i>Milad Ketab Ghale (Australian National University), Dirk Pattinson (Australian National University), and Michael Norrish (Data61, CSIRO, and ANU)</i>	
A Vision for Helping Developers Use APIs by Leveraging Temporal Patterns .95.....	95
<i>Erick Raelijohn (Université de Montréal), Michalis Famelis (Université de Montréal), and Houari Sahraoui (Université de Montréal)</i>	
A Proof-Producing Translator for Verilog Development in HOL .99.....	99
<i>Andreas Löw (Chalmers University of Technology Gothenburg) and Magnus O. Myreen (Chalmers University of Technology Gothenburg)</i>	
On the Formalization of Importance Measures Using HOL Theorem Proving .109.....	109
<i>Waqar Ahmad (Concordia University), Shahid Ali Murtza (National University of Sciences and Technology), Osman Hasan (National University of Sciences and Technology), and Sofiène Tahar (Concordia University)</i>	

Author Index 119	119
-------------------------------	-----