

# **2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI 2019)**

**Chambery, France  
18 – 21 June 2019**



**IEEE Catalog Number: CFP19SPI-POD  
ISBN: 978-1-5386-8343-9**

**Copyright © 2019 by the Institute of Electrical and Electronics Engineers, Inc.  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP19SPI-POD
ISBN (Print-On-Demand):	978-1-5386-8343-9
ISBN (Online):	978-1-5386-8342-2

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## TECHNICAL PROGRAM: ORAL PAPERS

### Session 1 - Modeling and Design Flow for SI/PI

[Performance Metrics for Crosstalk on Printed Circuit Boards in Frequency Domain](#) - K. Scharff, H.-D. Bruns and C. Schuster - Institute of Electromagnetic Theory, Hamburg University of Technology, Hamburg, Germany.....1

[Prediction of Frequency Dependent Shielding Behavior for Ground Via Fences in Printed Circuit Boards](#) - T. Hillebrecht, D. Dahl and C. Schuster - Institute of Electromagnetic Theory, Hamburg University of Technology (TUHH), Hamburg, Germany.....5

[Package Design Methodology for Crosstalk Mitigation between DC/DC Converter and ADC Analog Inputs in Complex SoC](#) - F. Settino<sup>1,2</sup>, T. Brandtner<sup>1</sup>, J. Nieder<sup>1</sup>, F. Praemassing<sup>1</sup>, H. Koffler<sup>1</sup>, P. Palestri<sup>3</sup>, F. Crupi<sup>2</sup> - <sup>1</sup>Infineon Technologies Austria; <sup>2</sup>DIMES, University of Calabria, Italy; <sup>3</sup>DPIA, University of Udine, Italy.....9

[A Novel Programmable Delay Line for VLSI Systems](#) - A. Bal<sup>1</sup>, J.N. Tiwari<sup>1</sup>, J.N. Tripathi<sup>1</sup>, R. Achar<sup>2</sup> - <sup>1</sup>STMicroelectronics, Greater Noida, India; <sup>2</sup>Carleton University, Ottawa, Canada.....13

### Session 2 (Special) - Emerging Substrate Integrated Technology

[A Review of Compact Substrate Integrated Waveguide \(SIW\) Interconnects and Components](#) - M. Bozzi<sup>1</sup>, L. Perregrini<sup>1</sup> and C. Tomassoni<sup>2</sup> - <sup>1</sup>Dept. of Electrical, Computer and Biomedical Engineering, University of Pavia, Italy; <sup>2</sup>Department of Engineering, University of Perugia, Italy.....16

[Low Loss SISL Patch-Based Coupler with Arbitrary Coupling Coefficient](#) - Y. Wang<sup>1</sup> and K. Ma<sup>2</sup> - <sup>1</sup>School of Physics, University of Electronic Science and Technology of China, Chengdu; <sup>2</sup>School of Microelectronics, Tianjin University, China.....20

[Passive Opto-Antenna using Air-Filled Substrate-Integrated-Waveguide Technology](#) - O. Caytan<sup>1</sup>, L. Bogaert<sup>1,2</sup>, H. Li<sup>1</sup>, J. Van Kerrebrouck<sup>1</sup>, S. Lemey<sup>1</sup>, J. Bauwelinck<sup>1</sup>, P. Demeester<sup>1</sup>, G. Torfs<sup>1</sup>, D. Vande Ginste<sup>1</sup> and H. Rogier<sup>1</sup> - <sup>1</sup>IDLab, Department of Information Technology, Ghent University; <sup>2</sup>Photonics Research Group, Department of Information Technology, Ghent University/imec.....24

[Use of Multilayered-PCB for Q-band Substrate Integrated Waveguide Components](#) - A. El Mostrah<sup>1</sup>, A. Manchec<sup>1</sup>, Y. Clavet<sup>1</sup>, and M. Cariou<sup>2</sup>, M. Sanchez-Soriano<sup>2</sup>, C. Quendo<sup>2</sup>, B. Potelon<sup>2</sup> - <sup>1</sup>Elliptika, Brest, France; <sup>2</sup>Univ Brest, Lab-STICC, CNRS, UMR 6285, Brest, France.....28

[Recent Advances in Filter Design Using The AFSIW Technological Platform](#) - T. Martin<sup>1,2,3</sup>, A. Ghiotto<sup>1</sup> and T.-P. Vuong<sup>3</sup> - <sup>1</sup>IMS, Univ. Bordeaux, France ; <sup>2</sup>Cobham Microwave, Cobham plc, Gradignan, France ; <sup>3</sup>IMEP-LAHC, Grenoble, France.....31

### Session 3 - Stochastic / Sensitivity Analysis

[A Hierarchical Approach to the Stochastic Analysis of Transmission Lines via Polynomial Chaos](#) - P. Manfredi and R. Trincherio - Department of Electronics and Telecommunications, Politecnico di Torino, Italy.....33

[Statistical Analysis of the Efficiency of an Integrated Voltage Regulator by means of a Machine Learning Model Coupled with Kriging Regression](#) - R. Trincherio<sup>1</sup>, M. Larbi<sup>2</sup>, M. Swaminathan<sup>2</sup> and F. G. Canavero<sup>1</sup> - <sup>1</sup>EMC Group, Department of Electronics and Telecommunications, Politecnico di Torino, Italy; <sup>2</sup>School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA.....37

### Session 4 - Macromodeling and Model Order Reduction

[On stabilization of parameterized macromodeling](#) - A. Zanco, S. Grivet-Talocia, T. Bradde and M. De Stefano - Dept. Electronics and Telecommunications, Politecnico di Torino, Italy.....41

[An IBIS-like Modelling for Power/Ground Noise Induced Jitter under Simultaneous Switching Outputs \(SSO\)](#) - M. Souilem<sup>1,4</sup>, J. N. Tripathi<sup>2</sup>, W. Dghais<sup>3,4,5</sup> and H. Belgacem<sup>3,4</sup> - <sup>1</sup>Ecole Nationale d'Ingénieurs de Sousse, <sup>3</sup>Institut Supérieur des Sciences Appliquées et de Technologie, Université de Sousse, Tunisia; <sup>2</sup>STMicroelectronics Pvt. Ltd., Noida, India; <sup>4</sup>Laboratory of Elec. and Microelec. Université de Monastir, Tunisia; <sup>5</sup>Laboratoire d'Ingénierie des Systèmes Industriels et des Energies Renouvelables, ENSIT, Tunis.....45

[A Bayesian Approach to Adaptive Frequency Sampling](#) - S. De Ridder, D. Deschrijver, D. Spina, T. Dhaene and D. V. Ginste - IDLab, Department of Information Technology, Ghent University-imec, Belgium.....49

[On the Extension of the TurboMOR-RC Reduction Method to RLC Circuits](#) - F. Bekmambetova and P. Triverio - The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Canada.....53

[A Wide-Band Equivalent Circuit Model for Single Slot Defected Ground Structures](#) - E. V. Nechel<sup>1</sup>, F. Ferranti<sup>2</sup>, Y. Rolain<sup>1</sup> and J. Lataire<sup>1</sup> - <sup>1</sup>Department of Fundamental Electricity and Instrumentation, Vrije Universiteit Brussel, Belgium; <sup>2</sup>Microwave Dept., IMT Atlantique, Lab-STICC, Brest, France.....57

### Session 5 - Electro-Magnetic Compatibility

[Finite element analysis of cable shields to investigate the behavior of the transfer impedance with respect to fast transients](#) - S. Bauer<sup>1</sup>, C. Türk<sup>2</sup>, W. Renhart<sup>1</sup> and O. Bíró<sup>1</sup> - <sup>1</sup>Institute of Fundamentals and Theory in Electrical Engineering, Graz, Austria; <sup>2</sup>Ministry of Defence of Austria, Vienna, Austria.....60

[Influence of Different Digital Power Supply Layout Styles on the EME of ICs with Respect to Process Variations](#) - A. Rauchenecker and T. Ostermann - Dept. Energy Efficient Analog Circuits and Systems, Institute for Integrated Circuits, JKU University of Linz, Austria.....64

[Study of the coupling of wide band Near Field Scan probe dedicated to the investigation of the radiated immunity of Printed Circuit Boards](#) - A. Durier<sup>1,2</sup>, S. Ben Dhia<sup>2</sup> and T. Dubois<sup>3</sup> - <sup>1</sup>MEA- CMR, IRT Saint Exupery, Toulouse, France; <sup>2</sup>ESE, LAAS-CNRS / INSA Toulouse, France; <sup>3</sup>IMS Bordeaux, France.....68

## Session 6 - Measurements and Characterization

[A Method to Determine Wide Bandgap Power Devices Packaging Interconnections](#) - L. Pace<sup>1,2</sup>, N. Defrance<sup>2</sup>, J-C. De Jaeger<sup>2</sup>, A. Videt<sup>1</sup> and N. Idir<sup>1</sup> -<sup>1</sup>Laboratory of Electrical Engineering and Power Electronics; <sup>2</sup>IEMN, University of Lille, France.....72

[Turnkey Methodology for Characteristic Impedance Extraction of Embedded Transmission Lines](#) - G. Houzet, P. Artillan, C. Bermond, T. Lacrevez and B. Flechet – IMEP-LaHC, University Savoie Mont-Blanc, Le Bourget du Lac, France.....76

## Session 7 - Interconnect Design and Optimization

[Mode Conversion Due To Residual Via Stubs in Differential Signaling](#) - J. Cedeno-Chaves<sup>1</sup>, K. Scharff<sup>2</sup>, A. Carmona-Cruz<sup>1</sup>, H.-D. Bruns<sup>2</sup>, R. Rimolo-Donadio<sup>1</sup> and C. Schuster<sup>2</sup> – <sup>1</sup>Department of Electronics Engineering, ITCR, Cartago, Costa Rica; <sup>2</sup>Institut für Theoretische Elektrotechnik, TUHH, Hamburg, Germany.....80

[Thermal and Signal Integrity Analysis of Novel 3D Crossbar Resistive Random Access Memories](#) - F. Zayer<sup>1,2,3</sup>, K. Lahbacha<sup>1</sup>, W. Dghais<sup>1,3</sup>, H. Belgacem<sup>1,3</sup>, M. de Magistris<sup>4</sup>, A. V. Melnikov<sup>5</sup>, A. Maffucci<sup>6,7</sup> - <sup>1</sup>Laboratory of Elec. and Microelec., <sup>2</sup>National Eng. School of Monastir, Tunisia; <sup>3</sup>Higher Inst. of Applied Science and Technology of Sousse, University of Sousse, Tunisia; <sup>4</sup>Dep. Electrical Eng. & Inform. Techn. University of Naples Federico II, Italy; <sup>5</sup>Institute for Nuclear Problems, Belarusian State University, Minsk, Belarus; <sup>6</sup>Dept of Electrical and Information Engineering, Univ. of Cassino and Southern Lazio, Italy; <sup>7</sup>INFN, Institute for Nuclear Physics, Frascati, Italy.....84

[Analysis of Jitter for a Chain-of-Inverters including On-chip Interconnects](#) - M. Suhail Illikkal<sup>1</sup>, J. N. Tripathi<sup>2</sup>, H. Shrimali<sup>1</sup> and R. Achar<sup>3</sup> – <sup>1</sup>School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, India; <sup>2</sup>ST Microelectronics, Greater Noida, India; <sup>3</sup>Carleton University, Ottawa, Canada.....88

[Optimization of a Miniaturized Ethernet 10 Gbits/s 8 Conductors Interconnect for Harsh Environments](#) - Y. Boujmad<sup>1</sup>, P. Artillan<sup>1</sup>, C. Bermond<sup>1</sup>, O. Gavard<sup>2</sup>, M. Prudhom<sup>2</sup>, F. Khalili<sup>2</sup>, E. Husson-Charlet<sup>2</sup>, J.-P. Barbosa<sup>2</sup> and B. Flechet<sup>1</sup> - <sup>1</sup>IMEP-LaHC, Le Bourget du Lac, France; <sup>2</sup>Amphenol-Socapex, Thyez, France.....92

## Session 8 - Power Distribution Networks

[Understanding NAND AC Timing Parameters and How to Accurately Implement them in SI Simulation](#) - S. Mobin and P. Balachander - Western Digital Corporation, Milpitas, CA, USA.....96

[Power Delivery Network Pre-Layout Design Planning and Analysis Through Automated Scripting](#) - C. M. Smutzer, C. K. White, C. R. Haider, and B. K. Gilbert - Mayo Clinic, Special Purpose Processor Development Group (SPPDG), Rochester, MN USA.....100

[A Frequency-Dependent Target Impedance Method Fulfilling Both Average and Dynamic Voltage Drop Constraints](#) – J. Chen, M. Hashimoto - Dept. Information Systems Eng., Osaka University, Japan.....104

[Expert System Synthesis for Evolutionary Decoupling Capacitor Optimization](#) - D. N. De Araujo and J. Pingnot - Electronic Board Systems Division, Mentor, a Siemens Business, USA.....108

## Session 9 - Microwave and mmWave Solutions for SiP and SoC

[RF line impedance optimization methodology in laminate technologies](#) - T. Monnier<sup>1</sup>, S. Danaie<sup>2</sup> and L. Schwartz<sup>3</sup> - <sup>1</sup>ADL – Silicon Packaging; FMT – <sup>2</sup>EWS Services; Grenoble, <sup>3</sup>BEMT R&D – Central Packaging, STMicroelectronics, Grenoble, France.....112

[Propagation Channel in Silicon in the Sub-THz Band for MPSoCs](#) - I. El Masri, T. Le Gouguec and P.-M. Martin - Univ Brest, Lab-STICC, Brest, France.....116

[Compact Analog All-Pass Phase-Shifter in 65-nm CMOS for 24/28 GHz on-Chip- and in-Package Phased-Array Antenna](#) - M. L. Carneiro<sup>1</sup>, M. Le Roy<sup>1</sup>, A. Pérennec<sup>1</sup>, R. Lababidi<sup>2</sup>, P. Ferrari<sup>3</sup> and V. Puyal<sup>4,5</sup> - <sup>1</sup>Univ Brest, Lab-STICC, Brest, France; <sup>2</sup>Ensta-Bretagne, Lab-STICC, Brest, France; <sup>3</sup>University of Grenoble Alpes, TIMA Laboratory, France; <sup>4</sup>University of Grenoble Alpes, Grenoble, France; <sup>5</sup>CEA, LETI, MINATEC campus, Grenoble, France.....120

### TECHNICAL PROGRAM: POSTER PAPERS

[CMOS Integrated PFM DC-DC Converter with Digitally-Controlled Frequency Selector](#) - Junho Yu, Seungki Jeon, Hoyong Choi, and Namsu Kim – School of ECE, Chungbuk National University, Cheong-ju, Korea.....124

[An Energy Efficient Spectrum Shaping Scheme for Substrate Integrated Waveguides](#) - Yu Zhao, R. Grünheid, G. Bauch – Institute of Communications, Hamburg University of Technology, Germany.....128

[Via Transition Optimization Using a Domain Decomposition Approach](#) – A. Carmona-Cruz<sup>1</sup>, K. Scharff<sup>2</sup>, J. Cedeño-Chaves<sup>1</sup>, H-D. Brüns<sup>2</sup>, R. Rimolo-Donadio<sup>1</sup> and C. Schuster<sup>2</sup> - <sup>1</sup>Department of Electronics Engineering, Instituto Tecnológico de Costa Rica (ITCR), Cartago, Costa Rica; <sup>2</sup>Institut für Theoretische Elektrotechnik, Technische Universität, Hamburg-Harburg, Germany.....132

[Transmission Line Design for Testing High-Speed Integrated Circuits with Differential Signals](#) – N. Bharat Thaker<sup>1</sup>, R. Ashok<sup>2</sup>, S. Manikandan<sup>2</sup>, N. Nambath<sup>3</sup>, S. Gupta<sup>2</sup> - <sup>1</sup>Silicon Photonics Product Division, Intel Technology India, Bengaluru, India; <sup>2</sup>Department of Electrical Engineering, IIT Bombay, Mumbai, India; <sup>3</sup>School of Electrical Sciences, IIT Goa, Ponda, India.....136

[Frequency-Domain Characterization of Power Inductors for Class-E Resonant Converters](#) – J. Bačmaga<sup>1</sup>, R. Blečić<sup>1</sup>, F. Pareschi<sup>2,3</sup>, R. Rovatti<sup>3,4</sup>, G. Setti<sup>2,3</sup>, A. Barić<sup>1</sup> - <sup>1</sup>Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy; <sup>2</sup>Advanced Research Center on Electronic Systems (ARCES), University of Bologna, Bologna, Italy; <sup>3</sup>Department of Electrical, Electronic and Information Engineering (DEI), University of Bologna, Bologna, Italy.....140

[Signal Quality Control for Cost-Effective Package Design](#) - Jisoo Hwang, Heeseok Lee, Hoi-Jin Lee and Youngmin Shin – Design Technology Team, System LSI Division, Samsung Electronics, Hwaseong-si, Korea.....144

[Modeling the Concentration Dependence for Manufacturing Single-Mode I/O Structures of MMI-Based Splitters in Thin Glass Sheets](#) - J.-P. Roth, T. Kühler and E. Griese – Theoretical Electrical Engineering and Photonics, University of Siegen, Germany.....148

[Open Defect Detection of Through Silicon Vias for Structural Power Integrity Test of 3D-Ics](#) – K. Hachiya<sup>1</sup>, A. Kurokawa<sup>2</sup> - <sup>1</sup>Faculty of Modern Life, Teikyo Heisei University, Tokyo, Japan; <sup>2</sup>Graduate School of Science and Technology, Hirosaki University, Japan.....152

[Power integrity Flow for mixed-signal NVM flash IP](#) – X. Lecoq<sup>1</sup>, A. Lipani<sup>2</sup>, S. Stemmer<sup>1</sup>, A. Chimeno<sup>3</sup> - <sup>1</sup>STMicroelectronics Grenoble, MDG division, Grenoble, France; <sup>2</sup>STMicroelectronics Palermo, MDG division, Palermo, Italy; <sup>3</sup>STMicroelectronics Crolles, TR&D division, Crolles, France.....156