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Invited Talk 1:

2019 Mar 19, 9:10 – 9: 40

Chair: Akio Higo, The University of Tokyo, Japan

 9:00
 Electronic photonic IC technology - challenges of on-wafer characterization and test

 Invited1
 [Invited]
 N/A

 Lars Zimmermann, IHP – Leibniz-Insitut für innovative Mikroelektronik, Germany

Session 1: Photonic Test Structures

2019 Mar 19, 9:40 - 11: 00

Co-Chairs: Alexey Kovalgin, University of Twente, The Netherland

- A Micro Racetrack Optical Resonator Test Structure to Optimize Pattern 9:40 1.1 Akio Higo¹, Tomoki Sawamura², Makoto Fujiwara¹, Etsuko Ota¹, Ayako Mizushima¹, Eric Lebrasseur¹, Taro Arakawa³, and Yoshio Mita^{1,2} ¹VLSI Design and Education Center, The University of Tokyo, Japan ²Graduate School of Engineering, The University of Tokyo, Japan ³Yokohama National University, Japan PbS Quantum Dot / ZnO Nanowires Hybrid Test Structures for Infrared 10:00 1.2 Haibin Wang¹, Akio Higo², Yoshio Mita³, Takaya Kubo¹, and Hiroshi Segawa^{1,4} ¹Research Center for Advanced Science and Technology, The University of Tokyo, Japan ²VLSI Design and Education Center, The University of Tokyo, Japan ³Graduate School of Engineering, The University of Tokyo, Japan ⁴Graduate School of Art and Science, the University of Tokyo, Japan In search of a hole inversion layer in Pd/MoOx/Si diodes through I-V characterization 10:20 1.3 Gaurav Gupta¹, Shivakumar D. Thammaiah^{1,2}, Raymond J.E. Hueting¹ and Lis K. Nanver^{1,2} ¹MESA+ Institute for Nanotechnology, University of Twente, The Netherlands ²Department of Materials and Production, Aalborg University, Denmark Wafer-Level Test Solution Development for a Quad-Channel Linear Driver Die in a 10:40
- 1.4
 400G Silicon Photonics Transceiver Module
 18

 Ye Wang, Hanyi Ding, Barry Blakely, Aidong Yan
 18

 Department of Silicon Photonics Test Development, GLOBALFOUNDRIES

SESSION 2: Yield & Reliability

2019 Mar 19, 11:20 – 12:20

Co-Chairs: Larg Weiland, PDF Solutions, USA Shigetaka Mori, SONY Corporation, Japan

11:20 Extracting BTI-induced Degradation without Temporal Factors by Using BTI-Sensitive

11:40 Extremely Low Voltage Operatable On-Chip-Monitor-Test Circuit for Plasma Induced

Invited Talk 2:

2019 Mar 19, 13:35 - 14:05

Chair: Tsuyoshi Sekitani, Osaka University, Japan

SESSION 3: Novel Process Characterization

2019 Mar 19, 14:05 - 15:25

Co-Chairs: Chadwin Young, University of Texas at Dallas

14:25 Continuity assessment for supercritical-fluids-deposited (SCFD) Cu film as

15:45 Test Structures for Characterising the Silver Chlorination Process During Integrated

¹School of Engineering, Institute for Integrated Micro and Nano Systems, The University of Edinburgh, UK

²School of Engineering, Institute for Bioengineering, The University of Edinburgh, UK

- 15:20 Test structure to assess the useful extent of regular dummy devices around

SESSION 4: Resistive Materials

2019 Mar 19 16:10 - 17:10

Co-Chairs: Stewart Smith, U. Edinburgh, UK Christopher Hess, PDF Solutions, USA

16:10	Resistance Measurement Platform for Statistical Analysis of Next Generation Memory
4.1	Materials
	Takeru Maeda ¹ , Yuya Omura ² , Akinobu Teramoto ³ , Rihito Kuroda ¹ , Tomoyuki Suwa ³ , and
	Shigetoshi Sugawa ^{1,3}
	¹ Graduate School of Engineering, Tohoku University, Japan
	² School of Engineering, Tohoku University, Japan
	³ New Industry Creation Hatchery Center, Tohoku University, Japan
16:30	Optimization of 36 Method for Phase-Change Materials Thermal Conductivity
4.2	Measurement at High Temperature
	Anna Lisa Serra, Guillaume Bourgeois, Marie Claire Cyrille, Jacques Cluzel, Julien Garrione,
	Gabriele Navarro and Etienne Nowak
	Univ. Grenoble Alpes, France
16:50	Evaluation of Truly Passive Crossbar Memory Arrays on Short Flow Characterization
4.3	Vehicle Test Chips
	Christopher Hess, Tomasz Brozek, Hendrik Schneider, Yuan Yu, Meindert Lunenborg
	Khim Hong Ng, Dennis Ciplickas, Rakesh Vallishayee, Christoph Dolainsky, Larg H. Weiland

PDF Solutions Inc., USA

17:10	Proposed one-dimensional	passive array test circu	it architecture for parallel kelvin
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4.4	measurement with efficient area use
	Matthew Rerecich ¹ , and Chadwin D. Young ²
	¹ Samsung Austin Semiconductor, LLC, USA
	² Materials Science and Engineering Department, University of Texas at Dallas, USA

Invited Talk 3:

2019 Mar 20, 09:00 - 09:30

Chair: Yoshio Mita, The University of Tokyo, Japan

09:00	Taming Emerging Devices' Variation and Reliability Challenges with Architectural
Invited3	and System Solutions [Invited]
	Yuyang Wang ¹ , Leilai Shao ¹ , Miguel Angel Lastras-Montaño ² , Kwang-Ting Cheng ³ ,
	¹ Department of Electrical and Computer Engineering, University of California, Santa
	Barbara, U.S.A.
	² Instituto de Investigación en Comunicación Óptica, FC, Universidad Autónoma de San
	Luis Potosí, México
	³ School of Engineering, Hong Kong University of Science and Technology, Hong Kong

SESSION 5: Power Device

2019 Mar 20 9:30 - 10:30

Co-Chairs: Tatsuya Ohguro, Toshiba, Japan

Vertical Bipolar Transistor Test Structure for Measuring Minority Carrier Lifetime in 9:30 5.1 K. Takeuchi¹, M. Fukui¹, T. Saraya¹, K. Itou¹, T. Takakura¹, S. Suzuki¹, Y. Numasawa², K. Kakushima³, T. Hoshii³, K. Furukawa³, M. Watanabe³, N. Shigyo³, H. Wakabayashi³, M. Tsukuda⁴, A. Ogura², K. Tsutsui³, H. Iwai³, S. Nishizawa⁵, I. Omura⁶, H. Ohashi³, and T. Hiramoto¹ ¹Institute of Industrial Science, the University of Tokyo, Japan ²Meiji University, Japan, ³Tokyo Institute of Technology, Japan ⁴*Green Electronics Research Institute, Japan*, ⁵*Kyushu University, Japan*, ⁶*Kyushu Institute of Technology, Japan* 9:50 Modeling and Test Structures for Accurate Current Sensing in Vertical Power FETs 5.2 Min Chu, Tikno Harjono, Kuntal Joardar, and Vijay Krishnamurthy

Advanced Technology Development, Texas Instruments, USA

10:10 A study on statistical parameter modeling of power MOSFET model by principal

SESSION 6: Matching & Variability

2019 Mar 20 10:50 - 12:10

Co-Chairs: Hans P. Tuinhout, *NXP Semiconductor, The Netherlands* Yuzo Fukuzaki, *Sony Corporation*

10:50	Two-transistor Voltage-Measurement-Based Test Structure for Fast Extraction of MOS	
6.1	Mismatch Design Parameters	
	Juan Pablo Martinez Brito ^{1,2} , Sergio Bampi ¹	
	¹ Graduate Program on Microelectronics - PGMICRO, Brazil	
	¹ Federal University of Rio Grande do Sul – UFRGS, Brazil	
	² CEITEC S.A. Semiconductors, Brazil	
11:10	On-Chip Threshold Voltage Variability Detector Targeting Supply of Ring Oscillator for	
6.2	Characterizing Local Device Mismatch	
	Poorvi Jain and Bishnu Prasad Das	
	Department of ECE, Indian Institute of Technology, India	
11:30	Comparison of MOSFET Threshold Voltage Extraction Methods with Temperature	
6.3	Variation	
	Yu-Hsing Cheng, Corporate Research and Development, ON Semiconductor, USA	
11:50	Analysis of Test Structure Design Induced Variation in on Si On-wafer TRL Calibration	
6.4	in sub-THz	
	Chandan Yadav, Sebastien Frégonèse, Marina Deng, Marco Cabbia, Magali De Matos,	
	Mathieu Jaoul, Thomas Zimmer	
	IMS Laboratory, University of Bordeaux, France	

SESSION 7: Measurement Technique

2019 Mar 20 13:30 - 15:10

Co-Chairs: Francesco Driussi, University of Udine – DPIA, Italy Bill Verzi, Keysight, USA

13:30	A Study of Power Supply Stability in Ring Oscillator Structures
7.1	Brad Smith ¹ , Donald Hall ¹ , Bill Verzi ² , and Dan Pechonis ¹
	¹ NXP Semiconductors, Austin, Texas, USA
	² Keysight Technologies, Austin, Texas, USA
13:50	Fast Tera-Ohm Measurement Approach Using V93k AVI64 DC Scale Card 142
7.2	Joern Stolle ¹ , Regis Poirier ² , Martin Froehle ³ , Hermann Weindl ³ , Martin Naiman, and Veit
	Kriegerstein ³
	¹ Advantest Europe GmbH, Boeblingen, Germany, ² Innova-test, Bordeaux, France,
	³ GLOBALFOUNDRIES, Dresden, Germany
14:10	A Study of Test Throughput Analysis on Capacitance Measurement of Parallel Test
7.3	Structures Using LCR and Direct Charge based Instruments
	Veenadhar Katragadda ¹ , Namita Deshmukh ¹ , Arthur Gasasira ¹ , Cheng-Mao Lee ² , Alan
	Cusick ¹
	¹ PDYE Test & Char, GlobalFoundries, USA
	² Semiconductor Test, Keysight Technologies, USA
14:30	Characterization and Modeling of Zener Diode Breakdown Voltage Mismatch
7.4	Man Yang ¹ , Colin C. McAndrew ² , Lei Chao ¹ , and Kejun Xia ¹
	¹ NXP Semiconductors, PRC, ² NXP Semiconductors, USA
14:50	Physical, small-signal and pulsed thermal impedance characterization of multi-finger
7.5	SiGe HBTs close to the SOA edges
	Marine Couret ¹ , Gerhard Fischer ² , Sebastien Frégonèse ¹ , Thomas Zimmer ¹ , Cristell Maneux ¹
	¹ IMS Laboratory, University of Bordeaux, France
	² IHP – Leibniz-Insitut für innovative Mikroelektronik, Germany

SESSION 8: Noise

2019 Mar 20 15:30 – 16:30

- Co-Chairs: Kiyoshi Takeuchi, *The University of Tokyo, Japan* Hirofumi Shinohara, *Waseda University, Japan*
- 15:30 Experimental Extraction of Body Bias Dependence of Low Frequency Noise in
- 8.1 sub-micron MOSFETs from Subthreshold to Moderate Inversion Regime 162 Chika Tanaka¹, Kanna Adachi², Atsushi Nakayama¹, Yasuhiko Iguchi¹, and Sadayuki Yoshitomi¹

¹Design Technology Innovation Division, Toshiba Memory Corporation ²Device Technology Research & Development Center, Institute of Memory Technology Research & Development, Toshiba Memory Corporation 15:50 Effect of Logic Depth and Switching Speed on Random Telegraph Noise Induced Delay

SESSION 9: Packaging

2019 Mar 21 9:20 - 10:20

Co-Chairs: Satoshi Habu, Keysight, Japan

- **9:20 Probing impact on pad moisture tightness: a challenge for pad size reduction** 176
- 9.1 Matthias Vidal-Dhô^{1,2}, Quentin Hubert¹, Patrice Gonon², Philippe Delorme¹, Jonathan Jacquot¹, Maxime Marchetti¹, Ludovic Beauvisage¹, Jean-Michel Moragues¹, Pascale Potard¹, Pascal Fornara¹, Jean-Philippe Escales¹, Pascal Sallagoity¹, Olivier Pizzuto¹, Delphine Maury¹, Jean-Michel Mirabel¹

¹STMicroelectronics Rousset, France, ²LTM CNRS, France

FormFactor Inc., Singapore

9.3 Yuki Okamoto¹, Ayako Mizushima², Naoto Usami¹, Jun Kinoshita³, Akio Higo², and Yoshio Mita¹

¹School of Electrical Engineering, The University of Tokyo

²VLSI Design & Education Center (VDEC), The University of Tokyo

³NEXTY Electronics Corporation

SESSION 10: TFTs

2019 Mar 21 10:40 - 11:20

Co-Chairs: Yoshio Mita, The University of Tokyo, Japan

- 10:40 Understanding the Effects of Low-Temperature Passivation and Annealing on ZnO

Michiaki Saito¹, Michihiro Shintani², Kazunori Kuribara³, Yasuhiro Ogasahara³, and Takashi Sato¹

¹Graduate School of Informatics, Kyoto University, Japan

²Graduate School of Science and Technology, Nara Institute of Science and Technology, Japan

³National Institute of Advanced Industrial Science and Technology (AIST), Japan