20th International Symposium on Quality Electronic Design (ISQED 2019)

Santa Clara, California, USA
6-7 March 2019

IEEE Catalog Number: CFP19250-POD
ISBN: 978-1-7281-0393-8

Copyright © 2019 by the Institute of Electrical and Electronics Engineers, Inc.
All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP19250-POD
ISBN (Print-On-Demand):	978-1-7281-0393-8
ISBN (Online):	978-1-7281-0392-1
ISSN:	1948-3287

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

TABLE OF CONTENTS

INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN 2019

WELCOME to ISQED 2019 iii

ISQED Committees iv

ISQED Best Paper of 2019 ix

General Information and Convention Center Floor Plan xi

Program at a Glance xiv

Keynote and Luncheon Speakers; Panel xv

Embedded Tutorials xix

SESSION 1A: Machine Learning in Conventional and Emerging Platforms

Chair: Prof. Ronald DeMara, University of Central Florida

Co-Chair: Dr. Sicheng Li, HPE

kNN-CAM: A k-Nearest Neighbors-based Configurable Approximate Floating Point Multiplier 1

Ming Yan, Yuntao Song, Yiyu Feng, Ghasem Pasandi, Massoud Pedram, Shahin Nazarian, University of Southern California

Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficien cy, and Power-Intermittency Resilience 8

Arman Roohi, Shaahin Angizi, Deliang Fan, Ronald F DeMara, University of Central Florida

Towards Collaborative Intelligence Friendly Architectures for Deep Learning 14

Amir Erfan Eshratifar, Amirhossein Esmaili, Massoud Pedram, University of Southern California

A General Framework to Map Neural Networks onto Neuromorphic Processor 20

Haowen Fang[1], Amar Shrestha[1], Ziyi Zhao[1], Yanzhi Wang[2], Qinru Qiu[1], [1]Syracuse University, [2]Northeastern University

SESSION 1B: Modern High-Level and Logic Synthesis

Chair: Srinivas Katkoori, University of South Florida

Co-Chair: Srini Krishnamoorthy, Apple

Approximate Logic Synthesis: A Reinforcement Learning-Based Technology Mapping Approach 26

Ghasem Pasandi, Shahin Nazarian, Massoud Pedram, University of Southern California

Fast Mapping-Based High-Level Synthesis of Pipelined Circuits 33

Chaofan Li[1], Sachin S. Sapatnekar[2], Jiang Hu[1], [1]Texas A&M University, [2]University of Minnesota

Characterization of Fast, Accurate Leakage Power Models for IEEE P2416 39

Barkha Gupta and W. Rhett Davis, North Carolina State University

Synthesis of Algorithm Considering Communication Structure of Distributed/Parallel Computing ... 45

Yukio Miyasaka[1], Ashish Mittal[2], Masahiro Fujita[1], [1]University of Tokyo, [2]Indian Institute of Technology Bombay

SESSION 1C: Emerging Memory and Spintronics Technologies for Future Energy Efficient Applications

Chair: Aswin Mehta, Texas Instruments

Co-Chair: Prof. Vita Hu, National Central University, Taiwan

Using Spin-Hall MTJs to Build an Energy-Efficient In-memory Computation Platform 52

Masoud Zabihi, Zhengyang Zhao, Mahendra DC, Zamshed I. Chowdhury, Salonik Resch, Thomas Peterson, Ulya R. Karpuzcu, Jian-Ping Wang, Sachin S. Sapatnekar, University of Minnesota

Low Restoration-Energy Differential Spin Hall Effect MRAM for High-Speed Nonvolatile SRAM Application 58
Sonal Shreya and Brajesh Kumar Kaushik, Indian Institute of Technology Roorkee

A Multi-Driver Write Scheme for Reliable and Energy Efficient 1S1R ReRAM Crossbar Arrays 64
Sherif Amer and Garrett Rose, University of Tennessee

Application of Probabilistic Spin Logic (PSL) in Detecting Satisfiability of a Boolean Function 70
Vaibhav Agarwal and Sneh Saurabh, Indraprastha Institute of Information Technology

SESSION 2A: Advances in Simulation, Design Optimization and Debug

Chair: Srini Krishnamoorthy, Apple
Co-Chair: Srinivas Katkoori, University of South Florida

A Compact Model of Negative Bias Temperature Instability Suitable for Gate-Level Circuit Simulation 76
Xu Liu[1], Alessandro Bernardini[2], Ulf Schlichtmann[2], Xing Zhou[1],
[1]Nanyang Technological University, [1]Technical University of Munich

An Automated Design Flow for Synthesis of Optimal Switching Power Supply 81
Pradeep Chawda[1], Anupriya Prasad[1], Kunjal Rathod[2], Kritika Solanki[3],
[1]Texas Instruments, [2]VMWare, Inc, [3]Chhattisgarh Swami Vivekanand Technical University

Robust Transistor Sizing for Improved Performances in Digital Circuits using Optimization Algorithms 85
Prateek Gupta, Harshini Mandadapu, Shirisha Gourishetty, Zia Abbas,
International Institute of Information Technology, Hyderabad

Resilient Reorder Buffer Design for Network-on-Chip 92
Zheng Xu[1] and Jacob Abraham[2], [1]ARM, Inc., [2]University of Texas at Austin

Simulation Based Assessment of SRAM Data Retention Voltage 98
Zhipeng Dong, Xi Cao, Ahosan Ul Karim, Vivek Joshi, Torsten Klick, Joerg Schmid, GLOBALFOUNDRIES

SESSION 2B: System Level Tools, Flows, Methods

Chair: Dr. Brajesh Kumar Kaushik, Indian Institute of Technology-Roorkee
Co-Chair: Swaroop Ghosh, Pennsylvania State University

Evaluating Design Space Subsetting for Multi-Objective Optimization in Configurable Systems 104
Mohamad Hammam Alsafrjalani[1], Tosiron Adegbija[2], Lokesh Ramamoorthi[1],
[1]University of Miami, [2]University of Arizona

A Scalable Image/Video Processing Platform with Open Source Design and Verification Environment 110
Xiaokun Yang[1], Yunxiang Zhang[1], Lei Wu[2], [1]University of Houston Clear Lake, [2]Auburn University at Montgomery

Power-aware IoT based Smart Health Monitoring using Wireless Body Area Network 117
Jitumani Sarma, Akash Katiyar, Rakesh Biswas, Hemanta Kumar Mondal,
Indian Institute of Information Technology, Guwahati

A Comprehensive Evaluation of Power Delivery Schemes for Modern Microprocessors 123
Jawad Haj-Yahya[1,4], Efraim Rotem[2], Avi Mendelson[3], Anupam Chattopadhyay[4],
[1]Nanyang Technological University, [2]Intel Corp, [3]Technion, Israel Institute of Technology,
[4]Agency for Science Technology and Research (ASTAR)

State Preserving Dynamic DRAM Bank Re-Configurations for Enhanced Power Efficiency 131
Kaustav Goswami[1], Hemanta Kumar Mondal[2], Shirshendu Das[3], Dip Sankar Banerjee[1],
[1]Indian Institute of Information Technology Guwahati, [2]National Institute of Technology Durgapur,
[3]Indian Institute of Information Technology Ropar

SESSION 2C: High Performance Application Specific Architecture

Chair: Shomit Das, AMD Research

Co-Chair: Aswin Mehta, Texas Instruments

Deterministic Stochastic Computation Using Parallel Datapaths 138
Alexander Groszewski and Travis Lenz, University of Texas at Austin

MAPIM: Mat Parallelism for High Performance Processing in Non-volatile Memory Architecture 145
Joonseop Sim[1], Minsu Kim[2], Yeseong Kim[1], Saransh Gupta[1], Behnam Khaleghi[1], Tajana Rosing[1],
[1]University of California San Diego, [2]University of Minnesota

Amoeba-Inspired Stochastic Hardware SAT Solver 151
Kazuaki Hara[1], Naoki Takeuchi[2], Masashi Aono[3], Yuko Hara-Azumi[1],
[1]Tokyo Institute of Technology, [2]Yokohama National University, [3]Keio University

Accelerating Deterministic Bit-Stream Computing with Resolution Splitting 157
M. Hassan Najafi[1], Sayed Abdolrasoul Faraji[1,2], Bingzhe Li[2], David Lilja[2], Kia Bazargan[2],
[1]University of Louisiana at Lafayette, [2]University of Minnesota

High-Performance NoCs Employing the DSP48E1 Blocks of the Xilinx FPGAs 163
Prabhu Prasad B M, Khyamling Parane, Basavaraj Talawar, National Institute of Technology Karnataka

SESSION 3A: Deep Learning Circuits and Architectures

Chair: Dr. Sicheng Li, HPE

Co-Chair: Pravin Kumar Venkatesan, Velodyne LiDAR

MReC: A Multilayer Photonic Reservoir Computing Architecture 170
Dharanidhar Dhang, Syed Ali Hasnain, Rabi Mahapatra, Texas A&M University

Dynamic Reconfiguration of CNNs for Input-Dependent Approximation 176
Maedeh Hemmat and Azadeh Davoodi, University of Wisconsin-Madison

An Application Specific Processor Architecture with 3D Integration for Recurrent Neural Networks 183
Sumon Dey and Paul D. Franzon, North Carolina State University

Task-Based Neuromodulation Architecture for Lifelong Learning 191
Anurag Reddy Daram[1], Dhireesha Kudithipudi[1], Angel Yanguas-Gil[2],
[1]Rochester Institute of Technology, [2]Argonne National Laboratory

SESSION 3B: Innovations In Classic Hardware Security Problems

Chair: Dr. Lin Yuan, Amazon

Co-Chair: Anupam Chattopadhyay, Nanyang Technological University

PUF-PassSE: A PUF based Password Strength Enhancer for IoT Applications 198
Qian Wang, Mingze Gao, Gang Qu, University of Maryland, College Park

On SAT-Based Attacks on Encrypted Sequential Logic Circuits 204
Yasaswy Kasarabada, Suyuan Chen, Ranga Vemuri, University of Cincinnati

A Darwinian Genetic Algorithm for State Encoding Based Finite State Machine Watermarking 210
Matthew Lewandowski and Srinivas Katkoori, University of South Florida

Lightweight Secure-Boot Architecture for RISC-V System-on-Chip 216
Jawad Haj-Yahya[1,2] Ming Ming Wong[1] Vikramkumar Pudi[1,3] Shivam Bhasin[1], Anupam Chattopadhyay[1],
[1]Nanyang Technological University, [2]Agency for Science Technology and Research (ASTAR),
[3]Indian Institute of Technology Tirupati

SESSION 3C: Co-Optimization of Device Performance and Design Reliability from State-of-the-art FinFET to Quantum Technologies

Chair: Prof. Vita Hu, National Central University, Taiwan
Co-Chair: Aswin Mehta, Texas Instruments

VeriSFQ: A Semi-formal Verification Framework and Benchmark for Single Flux Quantum Technology 224
Alvin D. Wong, Kevin Su, Hang Sun, Arash Fayyazi, Massoud Pedram, Shahin Nazarian, University of Southern California

Speed Optimization of Vertically Stacked Gate-All-Around MOSFETs with Inner Spacers for Low Power and Ultra-Low Power Applications 231
Ya-Chi Huang, Meng-Hsueh Chiang, Shui-Jinn Wang, National Cheng Kung University

Impact of Self-heating on Performance and Reliability in FinFET and GAAFET Designs 235
Vidya A. Chhabria and Sachin S. Sapatnekar, University of Minnesota

Device Designs and Analog Performance Analysis for Negative-Capacitance Vertical-Tunnel FET . 241
Hung-Han Lin and Vita Pi-Ho Hu, National Central University

SESSION 4A: Artificial Intelligence for Efficient Application Specific Hardware

Chair: Dr. Amey Kulkarni, Velodyne LiDAR
Co-Chair: Dr. Abhilash Goyal, Velodyne LiDAR

Behavioral Modeling of Tunable I/O Drivers with Pre-emphasis using Neural Networks 247
Huan Yu[1], Jaemin Shin[2], Tim Michalka[2], Mourad Larbi[1], Madhavan Swaminathan[1], [1]Georgia Institute of Technology, [2]Qualcomm Technologies, Inc.

Small Memory Footprint Neural Network Accelerators 253
Kenshu Seto[1], Hamid Nejatollahi[2], Jiyoung An[3], Sujin Kang[4], Nikil Dutt[2], [1]Tokyo City University, [2]University of California, Irvine, [3]Kyung Hee University, [4]Hanyang University

Minimizing Classification Energy of Binarized Neural Network Inference for Wearable Devices 259
Morteza Hosseini, Hirenkumar Paneliya, Utteja Kallakuri, Mohit Khatwani, Tinoosh Mohsenin, University of Maryland Baltimore County

Exploiting Energy-Accuracy Trade-off through Contextual Awareness in Multi-Stage Convolutional Neural Networks 265
KatayounNneshatpour, Farnaz Behnia, Houman Homayoun, Avesta Sasan, George Mason University

SESSION 4B: Verification, ATPG and Failure Analysis

Chair: Vinod Vishwanath, Real Intent, Inc.
Co-Chair: Sreejit Chakravarty, Intel Corporation

Assertion Coverage Aware Trace Signal Selection in Post-Silicon Validation 271
Xiaobang Liu and Ranga Vemuri, University of Cincinnati

A Communication-Centric Observability Selection for Post-Silicon System-on-Chip Integration Debug 278
Yuting Cao[1], Hao Zheng[1], Sandip Ray[2], [1]University of South Florida, [2]University of Florida

Automatic Test Pattern Generation for Double Stuck-at Faults based on Test Patterns of Single Faults 284
Peikun Wang, Amir Masoud Gharehbaghi, Masahiro Fujita, University of Tokyo

Deep Learning-Based Wafer-Map Failure Pattern Recognition Framework 291
Tsutomu Ishida, Izumi Nitta, Daisuke Fukuda, Yuzi Kanazawa, Fujitsu Laboratories Ltd.

SESSION 5A: Physical Design Optimization

Chair: Rung-Bin Lin, Yuan Ze University
Co-Chair: Srinivas Katkoori, Apple

Drive-Strength Selection for Synthesis of Leakage-Dominant Circuits **298**
Mahfuzul Islam[1], Shinichi Nishizawa[2], Yusuke Matsui[3], Yoshinobu Ichida[3],
[1]Kyoto University, [2]Saitama University, [3]ROHM Corporation

Estimating Pareto Optimum Fronts to Determine Knob Settings in Electronic Design Automation Tools **304**
Billy Huggins, W. Rhett Davis, Paul Franzon, North Carolina State University

An Artificial Intelligence Approach to EDA Software Testing: Application to Net Delay Algorithms in FPGAs **311**
Madhu Raman, Nizar Abdallah, Julien Dunoyer, Microsemi Corp.

Impact of Double-Row Height Standard Cells on Placement and Routing **317**
Rung-Bin Lin and Yu-Xiang Chiang, Yuan Ze University

SESSION 5B.1: 3D Integration & Advanced Packaging

Chair: Ali Arabi Ashahi, GlobalFoundries
Co-Chair: Vinod Vishwanath, Real Intent, Inc.

A Non-Slicing 3-D Floorplan Representation for Monolithic 3-D IC Design **323**
Shantonu Das and Dae Hyun Kim, Washington State University

Routing Complexity Minimization of Monolithic Three-Dimensional Integrated Circuits **329**
Sheng-En (David) Lin and Dae Hyun Kim, Washington State University

SESSION 5B.2: Future of SOC Architectures and Verification

Chair: Vinod Vishwanath, Real Intent, Inc.
Co-Chair: Ali Arabi Ashahi, GlobalFoundries

Towards Energy Efficient non-von Neumann Architectures for Deep Learning **335**
Antara Ganguly[1], Rajeev Muralidhar[2], Virendra Singh[1],
[1]Indian Institute of Technology Bombay, [2]Telstra Communications

Closing the Verification Gap with Static Sign-off **343**
Pranav Ashar and Vinod Viswanath, Real Intent, Inc.