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P. Evanschitzky, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); F. Shao, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany) and Erlangen Graduate School of Advanced Optical Technologies (Germany); T. Fühner, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); A. Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany) and Erlangen Graduate School of Advanced Optical Technologies (Germany)
- 7973 2A **Advanced scanner matching using freeform source and lens manipulators** [7973-82]
J.-H. Lim, K. Kang, S.-M. Kim, SAMSUNG Semiconductor (Korea, Republic of); W. Shao, F. Du, Z. Zhang, Z. Yu, J. Barbuto, V. Vellanki, Y. Cao, R. Goossens, Brion Technologies, Inc. (United States); S.-H. Park, C. K. Park, S. Hunsche, ASML Korea Co., Ltd. (Korea, Republic of); J. Lu, Brion Technologies Co., Ltd. (China)
- 7973 2B **Measurement of wavefront distortions in DUV optics due to lens heating** [7973-83]
K. Mann, A. Bayer, U. Leinhos, M. Schöneck, B. Schäfer, Laser-Lab. Göttingen e.V. (Germany)
- 7973 2C **Improved immersion scanning speed using superhydrophobic surfaces** [7973-84]
A. K. Gnanappa, E. Gogolides, NCSR Demokritos (Greece); E. Feuillet, F. Evangelista, N. Dziomkina, M. Riepen, ASML (Netherlands)
- 7973 2D **New 0.75 NA ArF scanning lithographic tool** [7973-85]
L. Duan, J. Cheng, G. Sun, Y. Chen, Shanghai Micro Electronics Equipment Co., Ltd. (China)
- 7973 2E **Simulation-based scanner tuning using FlexRay capability and scatterometry** [7973-111]
K. Bubke, GLOBALFOUNDRIES (Germany); M. Ruhm, ASML (Netherlands); R. Aldana, M. Niehoff, X. Xie, J. Ghan, Brion Technologies, Inc. (United States); P. van Adrichem, ASML (Germany); H. Bald, GLOBALFOUNDRIES (Germany); P. Luehrmann, ASML (Netherlands); S. Roling, R. Seltmann, GLOBALFOUNDRIES (Germany)

POSTER SESSION: MASK/WAFER TOPOGRAPHY, LAYOUT, AND OPC

- 7973 2F **Investigating the performance of directional boundary layer model through staged modeling method** [7973-87]
M.-G. Jeong, W.-C. Lee, S.-H. Yang, S.-H. Jang, S.-B. Shim, Y.-C. Kim, C. Suh, S.-W. Choi, Y.-H. Kim, SAMSUNG Electronics (Korea, Republic of)
- 7973 2G **Large scale model of wafer topography effects** [7973-88]
N. Voznesenskiy, Synopsys, Inc. (Estonia); H.-J. Stock, B. Kuchler, Synopsys GmbH (Germany); H. Song, J. Shiely, Synopsys, Inc. (United States); L. Bomholt, Synopsys Switzerland, LLC (Switzerland)
- 7973 2H **Study of model assisted rule base SRAF for random contact** [7973-89]
J. Moon, B.-S. Nam, C.-K. Kim, H.-S. Yun, Hynix Semiconductor Inc. (Korea, Republic of); J.-Y. Lee, Mentor Graphics (Korea, Republic of); D. Yim, S.-K. Park, Hynix Semiconductor Inc. (Korea, Republic of)
- 7973 2I **Physical simulation for verification and OPC on full chip level** [7973-90]
S. Shim, S. Moon, Y. Kim, S. Choi, Y. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of);

B. K uchler, U. Klostermann, Synopsys GmbH (Germany); M. Do, S. Lee, Synopsys Korea Inc. (Korea, Republic of)

- 7973 2J **Mask data correction methodology in the context of model-based fracturing and advanced mask models** [7973-91]
C. Pierrat, IC Images Technologies, Inc. (United States); L. Chau, I. Bork, D2S, Inc. (United States)
- 7973 2K **Optimizing OPC data sampling based on "orthogonal vector space"** [7973-92]
Y. Sun, Y. M. Foong, Y. Wang, J. Cheng, D. Zhang, S. Gao, N. Chen, B. I. Choi, GLOBALFOUNDRIES (Singapore); A. J. Bruguier, M. Feng, J. Qiu, S. Hunsche, L. Liu, W. Shao, Brion Technologies, Inc. (United States)
- 7973 2M **Tolerance-based OPC and solution to MRC-constrained OPC** [7973-94]
Y. Ping, X. Li, S. Jang, D. Kwa, Y. Zhang, R. Lugg, Synopsys, Inc. (United States)
- 7973 2N **Study of various RET for process margin improvement in 3X-nm DRAM contact** [7973-95]
H. Sim, H. Yune, Y. Ahn, J. Moon, B. Nam, D. Yim, S. Park, Hynix Semiconductor Inc. (Korea, Republic of)
- 7973 2O **A cost-driven fracture heuristics to minimize external sliver length** [7973-96]
X. Ma, S. Jiang, A. Zakhor, Univ. of California, Berkeley (United States)
- 7973 2P **A recursive cost-based approach to fracturing** [7973-97]
S. Jiang, X. Ma, A. Zakhor, Univ. of California, Berkeley (United States)
- 7973 2R **Full-chip OPC and verification with a fast mask 3D model** [7973-99]
H.-T. Huang, A. Mokhberi, Cadence Design Systems, Inc. (United States); H. Dai, C. Ngai, Applied Materials, Inc. (United States)
- 7973 2S **Overcome the process limitation by using inverse lithography technology with assist feature** [7973-100]
Y.-A. Shim, S. Jun, J. Choi, K. Choi, J. Han, Dongbu HiTek Co., Ltd. (Korea, Republic of); K. Wang, J. McCarthy, G. Xiao, G. Dai, D. Son, X. Zhou, T. Cecil, D. Kim, K. Baik, Luminescent Technology (United States)
- 7973 2T **Improvement on post-OPC verification efficiency for contact/via coverage check by final CD biasing of metal lines and considering their location on the metal layout** [7973-101]
Y. Kim, J.-Y. Choi, K. Choi, Dongbu HiTek (Korea, Republic of); J.-H. Choi, S.-R. Lee, Synopsys Inc. (Korea, Republic of)

POSTER SESSION: MODELING

- 7973 2V **Performance of a bilinear photoresist model** [7973-103]
A. Burov, M. Shi, J. Yan, W. Sun, Shanghai Micro Electronics Equipment Co., Ltd. (China)
- 7973 2W **Application of an inverse Mack model for negative tone development simulation** [7973-104]
W. Gao, Synopsys GmbH (Germany) and IMEC (Belgium); U. Klostermann, T. M lders, T. Schmoeller, W. Demmerle, Synopsys GmbH (Germany); P. De Bisschop, J. Bekaert, IMEC (Belgium)

- 7973 2X **A study of quantum lithography for diffraction limit** [7973-105]
S.-K. Kim, Hanyang Univ. (Korea, Republic of)
- 7973 2Y **Evaluating the performance of DP and EUVL by using analytical equations for resolution of optical lithography with considering required DOF** [7973-106]
M. Shibuya, K. Nogami, Tokyo Polytechnic Univ. (Japan); A. Takada, Topcon Corp. (Japan); S. Nakadate, Tokyo Polytechnic Univ. (Japan)

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- 7973 2Z **Lithography process control using focus and dose optimisation technique** [7973-108]
N. Spaziani, LTM/CNRS (France) and STMicroelectronics (France); R.-L. Inglebert, LTM/CNRS (France); J. Massin, STMicroelectronics (France)
- 7973 31 **Feasibility study on the mask compensation of gate CD non-uniformity caused by etching process** [7973-110]
W. H. Kim, E. J. Yet, S. I. Yet, B. C. Lee, X-FAB Sarawak Sdn. Bhd. (Malaysia)

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