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**Donis G. Flagello**

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E. C. Piscani, SEMATECH, Inc. (USA); S. Palmer, Texas Instruments (USA) and SEMATECH, Inc.  
(USA); C. Van Peski, SEMATECH, Inc. (USA)

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**POSTER SESSION: DEVELOPMENTS IN RET**

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- 652026 **Optical performance enhancement technique for 45-nm-node with binary mask** [6520-78]  
J.-S. Jung, H.-B. Kim, J.-W. Lee, S.-W. Choi, W.-S. Han, Samsung Electronics Co., Ltd. (South Korea)
- 652027 **Size tolerance of sub-resolution assist features for sub-50-nm node device** [6520-79]  
B.-S. Kim, S.-H. Lee, H.-J. Shin, N.-I. Lee, Samsung Electronics Co., Ltd. (South Korea)
- 652028 **A method for generating assist-features in full-chip scale and its application to contact layers of sub-70-nm DRAM devices** [6520-80]  
D.-W. Park, S. Kim, C. Hwang, S. Lee, H.-K. Cho, J.-T. Moon, Samsung Electronics Co., Ltd. (South Korea)
- 652029 **Process window optimization of CPL mask for beyond 45-nm lithography** [6520-82]  
S. Y. Tan, Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore)
- 65202A **SRAF placement and sizing using inverse lithography technology** [6520-83]  
T. Lin, Luminescent Technologies, Inc. (USA); F. Robert, A. Borjon, Crolles II Alliance (France); G. Russell, Luminescent Technologies, Inc. (USA); C. Martinelli, Crolles II Alliance (France); A. Moore, Luminescent Technologies, Inc. (USA); Y. Rody, Crolles II Alliance (France)
- 65202B **Optimal SRAF placement for process window enhancement in 65-nm/45-nm technology** [6520-84]  
C. Sarma, K. Herold, Infineon Technologies NA (USA); C. Noelscher, Qimonda Dresden GmbH & Co OHG (Germany); P. Schroeder, Infineon Technologies NA (USA)
- 65202C **Intensity weighed focus drilling exposure for maximizing process window of sub-100-nm contact by simulation** [6520-85]  
S. Jung, T.-C. Yang, T.-H. Yang, K.-C. Chen, C.-Y. Lu, Macronix International Co., Ltd. (Taiwan)
- 65202D **Process margin improvement using custom transmission EAPSM reticles** [6520-86]  
J. Buntin, S. Agarwal, B. Rolfson, R. Housley, B. Baggenstoss, E. Byers, Micron Technology Inc. (USA); C. Proglar, Photronics, Inc. (USA)
- 65202E **Verification of high-transmittance PSM with polarization at 193-nm high-NA system** [6520-88]  
C. F. Chiu, C. L. Chen, J. W. Lee, W. B. Wu, C. L. Shih, F. Y. Chen, J. P. Lin, NANYA Technology Corp. (Taiwan)

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**POSTER SESSION: DOUBLE PATTERNING AND EXPOSURE TECHNOLOGY**

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- 65202F **A litho-only approach to double patterning** [6520-20]  
A. Vanleenhove, D. Van Steenwinkel, NXP Semiconductors (Belgium)
- 65202H **A study of double exposure process design with balanced performance parameters for line/space applications** [6520-90]  
J. Zhu, Shanghai IC R&D Ctr. (China); P. Wu, Q. Wu, H. Ding, X. Li, C. Sun, NEC Electronics Co., Ltd. (China)

- 65202I **The improvement of photolithographic fidelity of two-dimensional structures through double exposure method** [6520-91]  
Q. Wenren, H. Ding, X. Li, C. Sun, Shanghai Huahong NEC Electronics Co., Ltd. (China); J. Zhu, Shanghai Integrated Circuit Research and Development Ctr. (China); Q. Wu, Shanghai Huahong NEC Electronics Co., Ltd. (China)
- 65202J **Double patterning with multilayer hard mask shrinkage for sub-0.25 k1 lithography** [6520-92]  
H. J. Liu, W. H. Hsieh, C. H. Yeh, J. S. Wu, H. W. Chan, W. B. Wu, F. Y. Chen, T. Y. Huang, C. L. Shih, J. P. Lin, Nanya Technology Corp. (Taiwan)
- 65202K **Sub-k1 = 0.25 lithography with double patterning technique for 45-nm technology node flash memory devices at  $\lambda = 193\text{nm}$**  [6520-93]  
G. Capetti, P. Cantù, E. Galassini, A. Vaglio Pret, C. Turco, A. Vaccaro, P. Rigolli, F. D'Angelo, G. Cotti, STMicroelectronics (Italy)
- 65202L **Quantum state control interference lithography and trim double patterning for 32-16 nm lithography** [6520-94]  
R. D. Frankel, B. W. Smith, A. Estroff, Rochester Institute of Technology (USA)
- 65202M **Double exposure using 193-nm negative tone photoresist** [6520-95]  
R. Kim, T. Wallow, J. Kye, H. J. Levinson, Advanced Micro Devices, Inc. (USA); D. White, TOK America, Inc. (USA)
- 65202N **Feasibility study of splitting pitch technology on 45-nm contact patterning with 0.93 NA** [6520-96]  
Y. F. Cheng, Y. L. Chou, T. C. Tseng, B. Y. Hsueh, C. H. Yang, United Microelectronics Corp. (Taiwan)
- 65202O **A study of process window capabilities for two-dimensional structures under double exposure condition** [6520-98]  
Q. Wu, P. Wu, Shanghai Huahong NEC Electronics Co., Ltd. (China); J. Zhu, Shanghai Integrated Circuit Research and Development Ctr. (China); H. Ding, X. Li, C. Sun, C. Peng, Shanghai Huahong NEC Electronics Co., Ltd. (China)
- 65202P **New double exposure technique without alternating phase-shift mask** [6520-99]  
T. Yamamoto, T. Yao, H. Futatsuya, T. Chijimatsu, S. Asai, Fujitsu Ltd. (Japan)
- 65202Q **ILT for double exposure lithography with conventional and novel materials** [6520-100]  
A. Poonawala, Univ. of California/Santa Cruz (USA); Y. Borodovsky, Intel Corp. (USA); P. Milanfar, Univ. of California/Santa Cruz (USA)

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**POSTER SESSION: EXPOSURE TOOLS, SUBSYSTEMS, AND MATERIALS**

- 65202R **Development and characterization of a 300-mm dual-side alignment stepper** [6520-101]  
W. W. Flack, E. M. True, R. Hsieh, D. Fuchs, R. Ellis, Ultratech, Inc. (USA)
- 65202T **Flare effect of different shape of illumination apertures in 193-nm optical lithography system** [6520-103]  
Y.-J. Yun, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea)

- 65202U **Silicon verification of flare model and application to real chip for long range proximity correction** [6520-104]  
D. Zhang, B. I. Choi, F. Y. Mei, S. T. Mulia, J. Y. Hsieh, Chartered Semiconductor Manufacturing Ltd. (Singapore); J. Word, Mentor Graphics Corp. (USA); Y. Yudhistira, Chartered Semiconductor Manufacturing Ltd. (Singapore)
- 65202V **Thermal aberration control for low-k1 lithography** [6520-105]  
Y. Uehara, T. Matsuyama, T. Nakashima, Y. Ohmura, T. Ogata, K. Suzuki, N. Tokuda, Nikon Corp. (Japan)
- 65202W **Quasi-telecentricity: the effects of unbalanced multipole illumination** [6520-106]  
S. P. Renwick, Nikon Precision, Inc. (USA)
- 65202X **Novel high-throughput micro-optical beam shapers reduce the complexity of macro-optics in hyper-NA illumination systems** [6520-107]  
T. Bizjak, T. Mitra, L. Aschke, LIMO Lissotschenko Mikrooptik GmbH (Germany)

### Part Three

- 65202Z **A solid-state 193-nm laser with high spatial coherence for sub-40-nm interferometric immersion lithography** [6520-109]  
A. J. Merriam, Actinix (USA); D. S. Bethune, J. A. Hoffnagle, W. D. Hinsberg, C. M. Jefferson, IBM Almaden Research Ctr. (USA); J. J. Jacob, Actinix (USA); T. Litvin, Kimoceo, Inc. (USA)
- 652030 **Investigations regarding the prevention of depolarization of ArF excimer laser irradiation by CaF<sub>2</sub> laser optics** [6520-110]  
U. Natura, D. Keutel, M. Letz, L. Parthier, K. Knapp, SCHOTT AG (Germany)
- 652031 **Reliable high-power injection locked 6kHz 60W laser for ArF immersion lithography** [6520-111]  
H. Watanabe, S. Komae, Gigaphoton Inc. (Japan); S. Tanaka, Ushio Inc. (Japan); R. Nohdomi, T. Yamazaki, H. Nakarai, J. Fujimoto, Gigaphoton Inc. (Japan); T. Matsunaga, Komatsu Ltd. (Japan); T. Saito, Gigaphoton inc. (Japan); K. Kakizaki, Ushio Inc. (Japan); H. Mizoguchi, Gigaphoton Inc. (Japan)
- 652032 **Increased availability of lithography light sources using advanced gas management** [6520-112]  
W. J. Dunstan, R. Jacques, K. O'Brien, A. Ratnam, Cymer, Inc. (USA)
- 652033 **A study of overlay mark robustness and enhanced alignment techniques for alignment improvement on metal layers of sub-100-nm technology** [6520-114]  
K. Dubey, T. Nakamura, Canon Singapore Pte., Ltd. (Singapore); H. Tanaka, N. Hayashi, S. Egashira, K. Mishima, T. Mase, T. Takeuchi, A. Honda, T. Kakizaki, Canon Inc. (Japan)
- 652034 **The optimization of zero-spaced microlenses for 2.2um pixel CMOS image sensor** [6520-115]  
H. Nam, J. L. Park, J. S. Choi, J. G. Lee, MagnaChip Semiconductor Inc. (South Korea)

- 652035 **Laser durability studies of high index immersion fluids: fluid degradation and optics contamination effects** [6520-197]  
V. Liberman, M. Rothschild, S. T. Palmacci, Lincoln Lab., Massachusetts Institute of Technology (USA); P. A. Zimmerman, A. Grenville, Intel Corp./International SEMATECH (USA)

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**POSTER SESSION: ILLUMINATION OPTIMIZATION AND CONTROL**

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- 652036 **Illumination optimization with actual information of exposure tool and resist process** [6520-116]  
K. Tsujita, K. Mikami, R. Naka, N. Baba, T. Ono, A. Suzuki, Canon Inc. (Japan)
- 652037 **Impact of illumination performance on hyper-NA imaging for 45-nm node** [6520-117]  
K.I. Mori, A. Yamada, T. Shiozawa, K. Takahashi, Canon Inc. (Japan)
- 652038 **Optimal solutions for the illuminator and final lens pupil coupled distributions beyond the axial symmetry** [6520-120]  
I. Ivonin, T. Sandstrom, Micronic Laser Systems AB (Sweden)
- 652039 **Sensitivity of hyper-NA immersion lithography to illuminator imperfections** [6520-122]  
W. Gao, SYNOPSIS, Inc. (Germany); L. De Winter, ASML Netherlands B.V. (Netherlands)

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**POSTER SESSION: IMAGE AND PROCESS MODELING**

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- 65203A **The calibration of process window model for 55-nm node** [6520-123]  
T. H. Wu, S. Y. Huang, C. W. Huang, P. R. Tsai, C. H. Yang, United Microelectronics Corp. (Taiwan); I. Y.-J. Su, Synopsys, Inc. (Taiwan); B. Falch, Synopsys, Inc. (USA)
- 65203B **SEM based data extraction for model calibration** [6520-124]  
M. Al-Imam, H. Y. Liao, J. Schacht, G. E. Bailey, Mentor Graphics Corp. (USA); T. H. Wu, C. W. Huang, S. Y. Huang, P. R. Tsai, C. H. Yang, United Microelectronics Corp. (Taiwan)
- 65203C **Distributed model calibration using Levenberg-Marquardt algorithm** [6520-125]  
M. Lu, L. Zhu, Grace Semiconductor Manufacturing Corp. (China); L. Ling, G. Zhang, Anchor Semiconductor Inc. (China); W. Chan, X. Zhou, Anchor Semiconductor Inc. (USA)
- 65203D **Analytical approach to high-NA images** [6520-126]  
S.-K. Kim, Catholic Univ. of Korea (South Korea) and Hanyang Univ. (South Korea)
- 65203E **Modeling and performance metrics for longitudinal chromatic aberrations, focus-drilling, and Z-noise: exploring excimer laser pulse-spectra** [6520-127]  
M. Smith, KLA-Tencor Corp. (USA); J. Bendik, Dynamic Intelligence Inc. (USA); I. Lalovic, N. Farrar, Cymer, Inc. (USA); W. Howard, C. Sallee, KLA-Tencor Corp. (USA)
- 65203F **Dr.LiTHO: a development and research lithography simulator** [6520-131]  
T. Fühner, T. Schnattinger, G. Ardelean, A. Erdmann, Fraunhofer Institute of Integrated Systems and Device Technology (Germany)
- 65203G **Lithographic characterization of evanescent-wave imaging systems** [6520-132]  
T. Graves, M. D. Smith, S. A. Robertson, KLA-Tencor Corp. (USA)

- 65203I **Heuristics for truncating the number of optical kernels in Hopkins image calculations for model-based OPC treatment** [6520-134]  
C. Zuniga, E. Tejnil, ASML Mask Tools Inc. (USA)

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**POSTER SESSION: IMAGE QUALITY AND CHARACTERIZATION**

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- 65203J **Topography induced defocus with a scanning exposure system** [6520-136]  
B. R. Liegl, IBM Microelectronics (USA); N. Felix, Cornell Univ. (USA); C. Brodsky,  
D. Dobuzinsky, IBM Microelectronics (USA)
- 65203K **Precise measurement of process bias and its relation to MEEF** [6520-139]  
T. E. Zavec, TEA Systems Corp. (USA)
- 65203L **Assessment of trade-off between resist resolution and sensitivity for optimization of hyper-NA immersion lithography** [6520-140]  
Y. Kishikawa, M. Kawashima, A. Ohkubo, Y. Iwasaki, S. Takeuchi, M. Yoshii, T. Honda, Canon Inc. (Japan)
- 65203M **Understanding the impact of rigorous mask effects in the presence of empirical process models used in optical proximity correction (OPC)** [6520-141]  
M. C. Lam, K. Adam, Mentor Graphics Corp. (USA)
- 65203N **Transistor-based electrical test structures for lithography and process characterization** [6520-142]  
W. J. Poppe, J. Holwill, L.-T. Pang, P. Friedberg, Q. Liu, L. Alarcon, A. Neureuther, Univ. of California/Berkeley (USA)
- 65203O **Use of starburst patterns in optical lithography** [6520-143]  
M. Burkhardt, IBM Research (USA); C. Tabery, Advanced Micro Devices Corp. (USA)
- 65203P **Challenging to meet 1-nm iso-dense bias (IDB) by controlling laser spectrum** [6520-144]  
T. Oga, Cymer, Inc. (Japan); T. Yamamoto, T. Yao, S. Asai, Fujitsu Limited (Japan); T. Kudo, T. Toki, Nikon Corp. (Japan)
- 65203Q **Impact of mask error on OPC for 45-nm node** [6520-145]  
O. Park, Infineon Technologies NA (USA)
- 65203R **Taking image quality factor into the OPC model tuning flow** [6520-147]  
C.-H. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)
- 65203S **Effects of laser bandwidth on iso-dense bias and line-end shortening at sub-micron process nodes** [6520-148]  
R. C. Peng, A. K. Yang, L. J. Chen, Y. W. Guo, H. H. Liu, J. Lin, TSMC Corp. (Taiwan);  
A. Chang, Cymer, Inc. (Taiwan)
- 65203T **On the quality of measured optical aberration coefficients using phase wheel monitor** [6520-149]  
L. V. Zavyalova, A. R. Robinson, A. Bourov, N. V. Lafferty, B. W. Smith, Rochester Institute of Technology (USA)

- 65203U **A comparative study for mask defect tolerance on phase and transmission for dry and immersion 193-nm lithography** [6520-150]  
M. L. Ling, National Univ. of Singapore (Singapore); G. S. Chua, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore); Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore)
- 65203V **The causes of horizontal-vertical (H-V) bias in optical lithography: dipole source errors** [6520-151]  
J. J. Biafore, KLA-Tencor Corp. (USA); C. A. Mack, Lithoguru.com (USA); S. A. Robertson, M. D. Smith, S. Kapasi, KLA-Tencor Corp. (USA)

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**POSTER SESSION: OPC AND IMPLEMENTATION**

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- 65203W **OPC-free on-grid fine random hole pattern formation utilizing double resist patterning with double RETs** [6520-153]  
S. Nakao, S. Maejima, T. Yamamoto, Y. Ono, J. Sakai, A. Yamaguchi, A. Imai, T. Hanawa, K. Sukoh, Renesas Technology Corp. (Japan)
- 65203X **Virtual OPC at hyper NA lithography** [6520-155]  
S. Lee, S.-W. Kim, Y.-J. Chun, S.-S. Suh, Y.-K. Jang, S.-J. Lee, S.-W. Choi, W.-S. Han, Samsung Electronics Co., Ltd. (South Korea)
- 65203Y **Mask-friendly OPC for a reduced mask cost and writing time** [6520-156]  
A. Yehia, Mentor Graphics Corp. (USA)
- 65203Z **Methods and factors to optimize OPC run-time** [6520-157]  
A. D. Dave, C. P. Babcock, S. N. McGowan, Y. Zou, Advanced Micro Devices, Inc. (USA)
- 652040 **Golden curve method for OPC signature stability control in high MEEF applications** [6520-158]  
K. Geidel, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany); T. Franke, Qimonda AG (Germany); S. Roling, AMD Fab 36 LLC and Co. KG (Germany); P. Buck, Toppan Photomasks, Inc. (USA); M. Sczyrba, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany); E. Mittermeier, Qimonda AG (Germany); R. Cinque, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany)
- 652041 **Mask enhancement using an evanescent wave effect (Best Student Paper Award)** [6520-159]  
N. V. Lafferty, J. Zhou, B. W. Smith, Rochester Institute of Technology (USA)
- 652042 **The gate CD uniformity improvement by the layout retarget with refer to the litho process** [6520-160]  
N.-Y. Chung, Y.-J. Yoon, S.-H. Lee, S.-I. Kim, S.-R. Ha, S.-Y. Lee, Samsung Electronics Co., Ltd. (South Korea)
- 652043 **Toward standard process models for OPC** [6520-161]  
Y. Granik, D. Medvedev, N. Cobb, Mentor Graphics Corp. (USA)
- 652044 **Modular process modeling for OPC** [6520-162]  
M. C. Keck, C. Bodendorf, T. Schmidting, Qimonda AG (Germany); R. Schlieff, Qimonda NA (USA); R. Wildfeuer, S. Zumpe, Qimonda GmbH and Co. OHG (Germany); M. Niehoff, Mentor Graphics Corp. (Germany)



- 652045 **Fast predictive post-OPC contact/via printability metric and validation** [6520-163]  
P. Yu, D. Z. Pan, The Univ. of Texas at Austin (USA)
- 652046 **Analysis of pattern density on process proximity compensation** [6520-165]  
S. Jung, F. Lo, T.-C. Yang, T.-H. Yang, K.-C. Chen, C.-Y. Lu, Macronix International Co., Ltd. (Taiwan)
- 652047 **Advanced new OPC method to improve OPC accuracy for sub-90-nm technology** [6520-166]  
J. Choi, J. Kang, Y. Shim, K. Yun, J. Hong, Y. Lee, K. Kim, Dongbu Electronics Co., Ltd. (South Korea)
- 652048 **Improving the model robustness for OPC by extracting relevant test patterns for calibration** [6520-168]  
M.-G. Jeong, S.-H. Lee, J.-E. Jung, C. Hyon, I. Choi, Y.-S. Kang, Y. Park, Samsung Electronics Co., Ltd. (South Korea)
- 65204A **Rapid search of the optimum placement of assist feature to improve the aerial image gradient in iso-line structure** [6520-170]  
J. Li, Q. Yan, L. S. Melvin III, Synopsys, Inc. (USA)
- 65204C **A feasible model-based OPC algorithm using Jacobian matrix of intensity distribution functions** [6520-172]  
Y. Chen, Zhejiang Univ. (China); K. Wu, Anchor Semiconductor, Inc. (USA); Z. Shi, X. Yan, Zhejiang Univ. (China)
- 65204D **Geometrical description of the microloading effect in silicon trench structures** [6520-173]  
I. Titarenko, E. Altshuler, R. Tweg, Tower Semiconductors, Ltd. (Israel)
- 65204E **Investigation of DFM-lite ORC approach during OPC simulation** [6520-174]  
C. T. Lim, K. Peter, V. Temchenko, D. Wallis, D. Kaiser, I. Meusel, S. Schmidt, Infineon Technologies Dresden GmbH and Co. OHG (Germany); M. Niehoff, Mentor Graphics Corp. (Germany)
- 65204F **Comparing traditional OPC to field-based OPC for 45-nm node production** [6520-175]  
R. Farnbach, J. Tuttle, M. St. John, R. Brown, D. Gerold, K. Lucas, R. Lugg, J. Shiely, M. Rieger, Synopsys, Inc. (USA)

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**POSTER SESSION: OPTIMIZATION, CONTROL, AND PERFORMANCE**

- 65204G **Studying the 3D mask effect on CD variation for 65-nm and beyond** [6520-176]  
C.-Y. Hung, Chartered Semiconductor Manufacturing (Singapore); Y. Gong, Jade Semiconductor, Ltd. (China)
- 65204H **CDU minimization at the 45-nm node and beyond: optical, resist, and process contributions to CD control** [6520-177]  
S. Scheer, M. Carcasi, Tokyo Electron America, Inc. (USA); T. Shibata, T. Otsuka, Tokyo Electron Kyushu Ltd. (Japan)
- 65204I **ACLV performance dry vs. immersion on 45-nm ground rules** [6520-179]  
U. P. Schroeder, Infineon Technologies NA (USA); C.-C. Yap, Chartered Semiconductors (USA); C. S. Sarma, Infineon Technologies NA (USA); A. Thomas, IBM Microelectronics (USA)

- 65204J **Feasibility study of 45nm metal patterning with 0.93 NA** [6520-181] Y. F. Cheng, Y. L. Chou, Y. C. Hou, B. J. Lu, C. H. Yang, United Microelectronics Corp. (Taiwan)
- 65204K **Optimization of DUV lithography for high-energy well implantation** [6520-182] R. Deschner, S.-D. Kim, R. Mann, M. Stidham, G. M. Johnson, J. Rolick, IBM Corp. (USA)
- 65204L **Challenges and solutions for transferring a 248-nm process to 365-nm imaging** [6520-183] A. Serebriakov, ASML Netherlands B.V. (Netherlands); C. Chang, SMIC (China); A. Becht, R. Pluijms, A. Cheng, E. Shi, H. van den Broek, L. Zhao, ASML Netherlands B.V. (Netherlands)
- 65204M **New color alignment for CMOS image sensor** [6520-184] M. K. Dagan, Tower Semiconductor, Ltd. (Israel); R. Edart, ASML Netherlands B.V. (Netherlands); H. Rechtman, Tower Semiconductor Ltd. (Israel); Y. Kanfi, P. Warnaar, ASML Netherlands B.V. (Netherlands); O. Moshe, Tower Semiconductor, Ltd. (Israel); R. van Haren, ASML Netherlands B.V. (Netherlands)
- 65204N **A thin FinFET Si-fin body structure fabricated with 193-nm scanner photolithography and composite hard mask etching technique upon bulk-Si substrate** [6520-185] W.-S. Liao, Y.-H. Liu, United Microelectronics Corp. (Taiwan); W.-T. Chang, United Microelectronics Corp. (Taiwan) and National Chia Tung Univ. (Taiwan); T.-H. Chen, T. Shih, H.-C. Tsen, L. Chung, United Microelectronics Corp. (Taiwan)
- 65204O **ARC stack development for hyper-NA imaging** [6520-186] V. Farys, STMicroelectronics (France); S. Warrick, Freescale Semiconductor (France); C. Chaton, CEA-LETI (France); J.-D. Chapon, STMicroelectronics (France)
- 65204P **A thick CESL stressed ultra-small (Lg=40-nm) SiGe-channel MOSFET fabricated with 193-nm scanner lithography and TEOS hard mask etching** [6520-187] W.-S. Liao, T.-H. Chen, H.-H. Lin, United Microelectronics Corp. (Taiwan); W.-T. Chang, United Microelectronics Corp. (Taiwan) and National Chia Tung Univ. (Taiwan); T. Shih, H.-C. Tsen, L. Chung, United Microelectronics Corp. (Taiwan)

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#### POSTER SESSION: PHOTOMASK TECHNOLOGY

- 65204Q **Three-dimensional mask effects and source polarization impact on OPC model accuracy and process window** [6520-188] M. Saied, Freescale Semiconductor (France); F. Foussadier, STMicroelectronics (France); J. Belledent, NXP Semiconductors (France); Y. Trouiller, CEA-LETI (France); I. Schanen, IMEP (France); C. Gardin, Freescale Semiconductor (France); J. C. Urbani, STMicroelectronics (France); P. K. Montgomery, Freescale Semiconductor (France); F. Sundermann, F. Robert, STMicroelectronics (France); C. Couderc, NXP Semiconductors (France); F. Vautrin, G. Kerrien, J. Planchot, STMicroelectronics (France); E. Yesilada, Freescale Semiconductor (France); C. Martinelli, STMicroelectronics (France); B. Wilkinson, Freescale Semiconductor (France); A. Borjon, L. Le-Cam, NXP Semiconductors (France); J. L. Di-Maria, CEA-LETI (France); Y. Rody, NXP Semiconductors (France); N. Morgana, Photronics, Inc. (USA); V. Farys, STMicroelectronics (France)
- 65204R **The choice of mask in consideration of polarization effects at high-NA system** [6520-189] S.-H. Kim, S.-H. Kim, S.-Y. Yu, Y.-H. Kim, J.-W. Lee, H.-K. Cho, Samsung Electronics Co., Ltd. (South Korea)

- 65204S **Analysis of diffraction orders including mask topography effects for OPC optimization** [6520-190]  
Y. Inazuki, N. Toyama, T. Adachi, T. Nagai, T. Suto, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

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**POSTER SESSION: POLARIZATION, HYPER-NA, AND IMMERSION LITHOGRAPHY**

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- 65204T **Immersion lithography with numerical apertures above 2.0 using high index optical materials** [6520-191]  
J. Zhou, N. V. Lafferty, B. W. Smith, Rochester Institute of Technology (USA); J. H. Burnett, NIST (USA)
- 65204U **Immersion defect reduction: I. Analysis of water leaks in an immersion scanner** [6520-193]  
F.-J. Liang, H. Chang, L.-H. Shiu, C.-K. Chen, L.-J. Chen, T.-S. Gau, B. J. Lin, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)
- 65204V **Defect testing using an immersion exposure system to apply immediate pre-exposure and post-exposure water soaks** [6520-194]  
R. D. Watso, T. Laursen, B. Pierson, K. D. Cummings, ASML (USA)
- 65204W **Polarization properties of state-of-art lithography optics represented by first canonical coordinate of Lie group** [6520-195]  
T. Fujii, Y. Kudo, Y. Ohmura, K. Suzuki, J. Kogo, Y. Mizuno, N. Kita, Nikon Corp. (Japan); M. Sawada, Nikon System (Japan)
- 65204X **Characteristics analysis of polarization module on optical proximity effect** [6520-196]  
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