
Processing Materials of 3D Interconnects, Damascene and Electronics Packaging

Editors:**K. Kondo**

Osaka Prefecture University
Osaka, Japan

F. Roozeboom

Eindhoven University of Technology
Eindhoven, The Netherlands

R. N. Akolkar

Intel Corporation
Hillsboro, Oregon, USA

M. Koyanagi

Tohoku University
Miyagi, Japan

D. Misra

New Jersey Institute of Technology
Newark, New Jersey, USA

Sponsoring Divisions:**Electrodeposition****Electronics and Photonics****Dielectric Science & Technology**

Published by

The Electrochemical Society

65 South Main Street, Building D
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

www.electrochem.org

ecs transactions™

Vol. 41, No. 43

Copyright 2012 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)
ISSN 2151-2051 (cd-rom)

ISBN 978-1-56677-985-2 (PDF)
ISBN 978-1-60768-344-5 (Softcover)

Printed in the United States of America.

ECS Transactions, Volume 41, Issue 43
Processing Materials of 3D Interconnects, Damascene and Electronics Packaging

Table of Contents

Preface	iii
---------	-----

**Chapter 1
Electroplating and Dielectrics**

Robust Ultrathin (20-25 nm)Trilayer Dielectric Low k Cu Damascene Cap for Sub-30 nm Nanoelectric Devices <i>S. V. Nguyen, T. Haigh Jr., M. Tagami, A. Grill, S. Cohen, H. Shobha, C. Hu, E. Adams, E. Liniger, T. Shaw, T. Cheng, H. Yusuff, Y. Xu, T. Ko, S. Molis, T. Spooner, S. Skordas, X. Liu, G. Bonilla, and D. Edelstein</i>	3
--	---

Evaluation of Grain Size Distributions of Cu Interconnects with Less Than 100nm Width by X-ray Diffraction Method <i>T. Inami and J. Onuki</i>	11
---	----

**Chapter 2
Electroplating**

(Invited) Resistivity Reduction in Very Narrow Cu Wiring <i>J. Onuki, Y. Sasajima, K. Tamahashi, K. YiQing, S. Terada, and K. Hidaka</i>	17
---	----

Electrolyte Additive Chemistry and Feature Size-Dependent Impurity Incorporation for Cu Interconnects <i>J. Kelly, T. Nogami, O. van der Straten, J. Demarest, J. Li, C. Penny, T. Vo, C. Parks, P. DeHaven, C. Hu, and E. Liniger</i>	23
---	----

Single Diallylamine Type Copolymer Additive which Perfectly Fills Cu Electrodeposition with only 1ppm <i>M. Takeuchi, K. Kondo, H. Kuri, M. Bunya, N. Okamoto, and T. Saito</i>	35
--	----

Chapter 3 TSV Filling

(Invited) High Speed Copper Electrodeposition for Through Silicon Via(TSV) <i>T. Hayashi, K. Kondo, M. Takeuchi, Y. Suzuki, T. Saito, N. Okamoto, M. Marunaka, T. Tsuchiya, and M. Bunya</i>	45
The Bottom-Up Copper Fill of Ø5µm × 40µm Vias Using 2-Component Model Chemistry <i>A. Radisic, L. Yang, C. Drijbooms, and H. Bender</i>	53
(Invited) Processing and Integration Considerations for Successful Copper Electrodeposition in 3D IC Applications <i>J. S. Papanu, M. Cogorno, and D. Erickson</i>	61
Conformal EL Ni Fill in Through-Silicon-Via for 3D Interconnects <i>C. S. Tiwari</i>	73
Laser Induced Forward Transfer of Interconnects for 3D Integration <i>G. Oosterhuis, A. Prenen, and A. Huis in't Veld</i>	81

Chapter 4 3D Manufacturing, Testing, and Reliability

Design and Verification of Benzocyclobutene (BCB) Templates for Chip-to-Wafer Alignment in 3D Integration <i>D. Zhang and J. Lu</i>	93
Removal Mechanism of Tungsten CMP Process: Effect of Slurry Abrasive Concentration and Process Temperature <i>Z. Wang, R. Peng, S. Xia, T. Kitajima, and S. Tsai</i>	103
Self-Controlled Constant-Current Temperature Stress for Triangular Voltage Sweep Measurements of Cu <i>I. Ciofi, M. Mannarino, Y. Li, K. Croes, and G. P. Beyer</i>	113
The Performance and Density Advantages of 3D FPGA <i>Y. Nakagawa, K. Osada, T. Matsumura, H. Koike, N. Miyamoto, and K. Takeda</i>	125
Author Index	135