Processing, Materials, and Integration of Damascene and 3D Interconnects

Editors:

J. Flake
Louisiana State University
Baton Rouge, Louisiana, USA

M. Koyangi
Tohoku University
Sendai, Japan

G. S. Mathad
S/C Technology Consulting
Poughkeepsie, New York, USA

H. S. Rathore
IBM
Stormville, New York, USA

T. Ritzdorf
Applied Materials/Semitool
Kalispell, Montana, USA

O. Leonte
Berkeley Polymer Technology
Hayward, California, USA

P. Ramm
Fraunhofer Institute IZM Münich
Münich, Germany

F. Roozeboom
Eindhoven University of Technology
Eindhoven, Netherlands

Sponsoring Divisions:

Electronics and Photonics

Dielectric Science & Technology

Published by
The Electrochemical Society
65 South Main Street, Building D
Pennington, NJ 08534-2839, USA
tel 609 737 1902
fax 609 737 2743
www.electrochem.org

ecs transactions ™

Vol. 33, No. 12

Copyright 2010 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)
ISSN 2151-2051 (cd-rom)

ISBN 978-1-56677-831-2 (PDF)
ISBN 978-1-60768-181-6 (Softcover)

Printed in the United States of America.

ECS Transactions, **Volume 33, Issue 12**
Processing, Materials, and Integration of Damascene and 3D Interconnects

Table of Contents

Preface iii

Integration and Frequency Dependent Parametric Modeling of Through Silicon via Involved in High Density 3D Chip Stacking 1
L. Cadix, C. Fuchs, M. Rousseau, P. Leduc, H. Chaabouni, A. Thuaire, M. Brocard, A. Valentian, A. Farcy, C. Bermond, N. Sillon, P. Ancey, and B. Fléchet

Modeling of Electromigration Induced Contact Resistance Reduction of Cu-Cu Bonded Interface 23
R. I. Made, C. Gan, and C. Tan

Leakage Current Analysis of Lateral p+/n Ge Based Diode Activated at Low Temperature for Three-Dimensional Integrated Circuit (3D-ICs) 35
W. Jung, J. Park, D. Kuzum, W. Kim, S. Wong, and K. C. Saraswat

Use of Polymer Liners for 3D-WLP TSVs: Process, Reliability and Cost 41
D. Sabuncuoglu Tezcan, N. Pham, B. Majeed, Y. Civale, and E. Beyne

From 2D Lithography to 3D Patterning 55
H. W. van Zeijl, J. Wei, C. Shen, T. M. Verhaar, and P. Sarro

3D Hybrid Integration Technology for Opto-Electronic Hetero-Integrated Systems 71
K. Lee, T. Fukushima, T. Tanaka, and M. Koyanagi

High-Performance 3D Interconnects Based on Electrochemical Etch and Liquid Metal Fill 91
H. Hedler, T. Scheiter, and M. Schieber

CMOS Compatible Anodization Process for Low Cost High Density Capacitors 107
M. Detalle, M. Rakowski, G. Potoms, A. Mercha, M. de Potter de ten Broeck, A. Phommahaxay, D. Sabuncuoglu Tezcan, and P. Soussan

Ultra Low-k Materials: Challenges of Scaling 117
L. Zhao, M. Baklanov, M. Pantouvaki, Z. Tőkei, and G. Beyer

Ultra-Low Temperature Deposition of Copper Seed Layers by PEALD 125
J. Mao, E. Eisenbraun, V. Omarjee, A. Korolev, C. Lansalot, and C. Dussarrat

Ultrathin (5-35 nm) SiCNH Dielectrics for Damascene Cu Cap Application: Thickness Scaling and Oxidation Barrier Performance Limitation 137
S. V. Nguyen, T. Haigh Jr., T. Shaw, S. Molis, C. Dziobkowski, C. Zahakos, S. Cohen, H. Shobha, E. Liniger, C. Hu, G. Bonilla, N. Klymko, and A. Grill

CMP for Cu Interconnect with Advanced Barrier Materials 147
Y. Wang, M. Gage, K. Xu, Y. Wang, Y. Chen, S. Xia, W. Tu, and L. Karuppiah

Subtractive Etching of Cu with Hydrogen-Based Plasmas 157
F. Wu, G. Levitin, and D. Hess

Author Index 163