
Thin Film Transistors 10 (TFT 10)

Editor:

Y. Kuo

Texas A&M University
College Station, Texas, USA

Sponsoring Division:

 **Electronics and Photonics**



Published by

The Electrochemical Society

65 South Main Street, Building D
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

www.electrochem.org

ecstransactions™

Vol. 33, No. 5

Copyright 2010 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)
ISSN 2151-2051 (cd-rom)

ISBN 978-1-56677-824-4 (Hardcover)
ISBN 978-1-60768-174-8 (PDF)

Printed in the United States of America.

Table of Contents

<i>Preface</i>	<i>iii</i>
Chapter 1 Devices Modeling, Scalability, and Reliability	
(Invited) Downscaling Issues in Polycrystalline Silicon TFTs <i>G. Fortunato, M. Cuscunà, P. Gaucci, L. Maiolo, L. Mariucci, A. Pecora, and A. Valletta</i>	3
(Invited) The Silicon Nanowire Accumulation-Mode MOSFETs <i>J. Wu, P. Garg, and S. Fonash</i>	23
(Invited) Stabilities of TFTs under Bias-Stress <i>J. Jang, M. Mativenga, and J. Choi</i>	31
(Invited) Reliability of Polycrystalline Silicon Thin-Film Transistors on the Glass Substrate <i>S. Choi and M. Han</i>	41
The AC-Bias Stability of Short Channel a-Si:H TFT <i>S. Park, S. Lee, J. Woo, J. Yoo, and M. Han</i>	51
Enhanced Performance and Thermal Stability of a-Si:H TFTs <i>A. Indluru and T. L. Alford</i>	57
The Influence of Electromechanical Stress on the Stability of Nanocrystalline Silicon Thin Film Transistors Made on Colorless Polyimide Foil <i>I. Chiu, J. Huang, Y. Chen, I. Cheng, J. Chen, and M. Lee</i>	65
The 1/f Noise Performance for TFTs Fabricated in Three TFT Technologies: Monocrystalline Silicon on Glass, Low Temperature Polysilicon on Glass, and Silicon on Insulator <i>S. A. Marshall, C. J. Nassar, J. Choi, J. Jang, C. Kosik Williams, E. Mozdy, T. J. Tredwell, and R. J. Bowman</i>	71

Reduction of Hot Carrier Effects in Corning Silicon-on-Glass TFTs <i>M. Mativenga, M. Choi, W. Choi, J. Choi, J. Jang, R. Mruthyunjaya, T. J. Tredwell, E. Mozdy, and C. Kosik Williams</i>	83
High Field Induced Stress Suppression of GIDL Effects in Accumulation-Mode P-Channel TFTs <i>A. McCabe, R. G. Manley, J. Couillard, C. Kosik Williams, and K. Hirschman</i>	95
Capacitance Model for Thin-Film Transistors with Interface Traps <i>H. Tsuji, Y. Kamakura, and K. Taniguchi</i>	105
A Charge Based Compact Modeling Technique for Monocrystalline TFTs on Glass <i>C. J. Nassar, T. J. Tredwell, C. Kosik Williams, J. Revelli, and R. J. Bowman</i>	111

Chapter 2 Materials

(Invited) A New Insulator for Thin-Film Transistor Backplanes and for Flexible Passivation Layers <i>L. Han, K. Song, S. Wagner, and P. Mandlik</i>	125
Characterization of Silicon-on-Glass Substrates Using Variable Angle Spectroscopic Ellipsometry <i>R. D. Rettmann, J. Couillard, and K. Hirschman</i>	135
Protection Layer Effects on the Device Performance of Oxide/Organic Hybrid TFTs <i>S. Yang, S. Ko Park, M. Ryu, D. Cho, C. Hwang, S. Yoon, C. Byun, K. Cho, O. Kwon, S. Kim, C. Park, and J. Jang</i>	143

Chapter 3 Si-based TFTs

(Invited) Nano-Inkjet and Its Application to Metal-Induced Crystallization of a-Si for Poly-Si TFTs <i>T. Asano and Y. Ishida</i>	149
Reducing Ni Residues of Metal Induced Crystallization Poly-Si with a Simple Chemical Oxide Layer <i>M. Lai and Y. S. Wu</i>	157

Using Fluorine-Ion Implanted a-Si Layer to Reduce Ni Contamination and Passivate the Defects in NILC Poly-Si <i>C. Chen and Y. S. Wu</i>	161
Improved Electrical Performance of NILC Poly-Si TFTs Manufactured Using H ₂ SO ₄ and HCl Solution <i>Y. Chen, Y. Chao, and Y. S. Wu</i>	165
Improved Performance of NILC Poly-Si Nanowire TFTs by Using Ni-Gettering <i>B. Wang, T. Yang, Y. S. Wu, C. Su, and H. Lin</i>	169
Electrical Characteristics of a Reduced-Gate Structure Polycrystalline Silicon Thin Film Transistor Using Field-Aided Lateral Crystallization <i>J. You, K. Lee, D. Choi, and Y. Kim</i>	173
(Invited) Polycrystalline Silicon Thin Film Transistors <i>T. Sameshima</i>	183
High Performance and Reliability of Poly-Si TFTs Using Nickel Drive-In Induced Lateral Crystallization <i>Y. S. Wu and C. Chang</i>	193
Characterization and Reliability of Gate-All-Around Poly-Si TFTs with Multinowire Channels <i>H. Liu, S. Chiou, C. Hung, and F. Wang</i>	197
(Invited) Nanocrystalline Silicon Thin Film Transistors <i>M. R. Rad, G. R. Chaji, C. Lee, D. Striakhilev, A. Sazonov, and A. Nathan</i>	205
High Performance Micro-Crystalline Silicon TFT Using Indirect Thermal Crystallization Technique <i>B. Choi, K. Kim, J. Bae, S. Lee, H. Lee, S. Kim, K. Park, C. Kim, Y. Hwang, and I. Chung</i>	213
Electrical and Mechanical Behaviors of Microcrystalline TFTs Deposited on PEN <i>S. Janfaoui, K. Kandoussi, C. Simon, N. Coulon, S. Crand, and T. Mohammed-Brahim</i>	217
Schottky Diode Based on Microcrystalline Silicon Deposited at 165°C for RFID Application <i>I. Souleiman, K. Kandoussi, K. Belarbi, C. Simon, N. Coulon, S. Crand, and T. Mohammed-Brahim</i>	227

Chapter 4 **Organic TFTs**

(Invited) Inkjet-Patterned, Organic Complementary Circuits Integrated with Polymer Mechanical Sensors	239
<i>T. Ng, J. Daniel, S. Garner, B. Krusor, B. Russo, and A. Arias</i>	
Influence of Bank Structure on the Film Morphology and Electrical Properties of Ink-Jet Printed TIPS Pentacene Thin-Film Transistors	245
<i>Y. Kim, M. Oh, S. Park, and M. Han</i>	
(Invited) Electrical and Environmental Stability of Organic Transistors	251
<i>J. Bedolla, J. Northrup, D. Belaineh, V. Wagner, and D. Knipp</i>	
Flow Rate's Influence on Low Temperature Silicon Oxide Deposited by Atmospheric Pressure Plasma Jet for Organic Thin Film Transistor Application	255
<i>K. Chang, S. Huang, and C. Cheng</i>	
Improved Performance of Pentacene OTFT with HfLaO Gate Dielectric by Annealing in NH ₃	265
<i>L. Deng, P. Lai, J. Xu, H. Choi, W. Chen, and C. Che</i>	

Chapter 5 **Metal Oxide TFTs**

Low Temperature, High-Performance, Solution-Processed Indium Oxide Based Thin Film Transistors	275
<i>S. Han, G. Herman, and C. Chang</i>	
Low Temperature Solution-Processed Zinc Tin Oxide Thin Film Transistor with O ₂ Plasma Treatment	283
<i>J. Lee, Y. Kim, Y. Lee, S. Cho, Y. Kim, J. Kwon, and M. Han</i>	
Solution-Processed Oxide Thin-Film Transistor with Spin-Coated Zinc Tin Oxide Active Layer and Indium Zinc Oxide Source/Drain Electrodes	289
<i>Y. Kim, J. Lee, Y. Lee, S. Cho, Y. Kim, and M. Han</i>	
Solution-Processed Oxide Thin Film Transistors with Indium Zinc Tin Oxide Semiconductor: Nitrogen Effect	295
<i>B. Kim, H. Kim, S. Jung, T. Yoon, Y. Kim, and H. Lee</i>	

The Electrical Properties of Atomic Layer Deposition of ZnO:N Thin Film Transistors by Ultraviolet Exposure <i>J. Kim, S. Lim, and H. Kim</i>	301
The Stability of Oxide TFTs under Electrical Gate Bias and Monochromatic Light Illumination <i>S. Lee, S. Kim, Y. Lee, S. Park, J. Kwon, and M. Han</i>	313
The Effect of Light Illumination on Transfer Curve and Stability of Amorphous Hf-In-ZnO Thin Film Transistors <i>J. Kim, U. Kim, Y. Chung, S. Rha, H. Jung, S. Lee, J. Jung, S. Lee, and C. Hwang</i>	319
The Effect of Illumination on the Negative Bias Temperature Instability in Zinc Tin Oxide Thin Film Transistors <i>U. Kim, J. Kim, H. Oh, Y. Chung, and C. Hwang</i>	325
Study of the Effect of Electrical Stress on ZnO TFTs <i>L. Su, H. Lin, S. Wang, Y. Yeh, C. Cheng, L. Peng, and J. Huang</i>	331
Improved Thermal Stability of Indium Zinc Oxide TFTs by Low Temperature Post Annealing <i>A. Indluru and T. L. Alford</i>	337
Characteristics of Zinc Oxide Thin Film Transistors Fabricated by Location-Controlled Hydrothermal Method <i>P. Yang, J. Wang, W. Tsai, S. Wang, P. Chen, N. Su, J. Lin, I. Lee, C. T. Chang, Y. Wei, and H. Cheng</i>	345

Chapter 6 **Memories**

(Invited) Mechanism and Performance of Floating-Gate a-Si:H TFT Nonvolatile Memory Devices <i>Y. Kuo</i>	357
High Retention-Time Nonvolatile Amorphous Silicon TFT Memory for Static Active Matrix OLED Display without Pixel Refresh <i>Y. Huang, B. Hekmatshoar, S. Wagner, and J. Sturm</i>	365
Amorphous Oxide Semiconductor Memory Using High-k Charge Trap Layer <i>S. Rha, J. Jung, J. Kim, U. Kim, Y. Chung, H. Jung, S. Lee, and C. Hwang</i>	375

Chapter 7
Advanced Applications

(Invited) Towards EPC Compatible Plastic RFID Tags	383
<i>K. Myny, S. Steudel, P. Vicca, S. Smout, M. Beenhackers, N. van Aerle, F. Furthner, B. van der Putten, A. Tripathi, G. Gelinck, J. Genoe, W. Dehaene, and P. Heremans</i>	
Low Voltage Driven CMOS Circuits Based on Silicon on Glass	391
<i>M. Choi, J. Choi, S. Park, W. Choi, M. Mativenga, J. Jin, R. Mruthyunjaya, T. J. Tredwell, E. Mozdy, and C. Kosik Williams</i>	
The Application of Organic Electrochemical Transistors in Biosensors	399
<i>F. Yan, P. Lin, and H. Chan</i>	
(Invited) Poly-Si TFT Based Technologies and Circuits for Multipurpose Sensors	409
<i>O. Bonnaud and T. Mohammed-Brahim</i>	
Polysilicon Source-Gated Transistors for Mixed-Signal Systems-on-Panel	419
<i>R. Sporea, X. Guo, J. Shannon, and S. Silva</i>	
Author Index	425