
ULSI Process Integration 8

Editors:**C. Claeys**

IMEC

Leuven, Belgium

H. Iwai

Tokyo Institute of Technology

Tokyo, Japan

M. TaoUniversity of Texas at Arlington
Arlington, Texas, USA**S. Deleonibus**

CEA-LETI

Grenoble, France

J. MurotaTohoku University
Sendai, Japan**Sponsoring Division:****Electronics and Photonics**

Published by

The Electrochemical Society65 South Main Street, Building D
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

www.electrochem.org

ecstransactions™**Vol. 58, No. 9**

Copyright 2013 by The Electrochemical Society.
All rights reserved.

This book has been registered with Copyright Clearance Center.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

ISSN 1938-6737 (online)
ISSN 1938-5862 (print)
ISSN 2151-2051 (cd-rom)

ISBN 978-1-62332-100-0 (Hardcover)
ISBN 978-1-60768-454-1 (PDF)

Printed in the United States of America.

Table of Contents

<i>Preface</i>	<i>iii</i>
----------------	------------

**Chapter 1
Keynote Presentations**

FDSOI Technology: A Power Efficient Solution Down to 10nm <i>O. Faynot, M. Vinet, C. Fenouillet, O. Weber, P. Perreau, L. Grenouillet, F. Andrieu, T. Poiroux, S. Deleonibus</i>	3
Memristive Devices for Computing: Mechanisms, Applications and Challenges <i>J. J. Yang, B. J. Choi, M. X. Zhang, A. C. Torrezan, J. P. Strachan, R. S. Williams</i>	9

**Chapter 2
Back-end Processing**

(Invited) Low Temperature Direct Bonding 3D Stacking Technologies for High Density Device Integration <i>L. Di Cioccio, I. Radu, G. Gaudin, T. Lacave, F. Baudin, M. Sadaka, T. Signamarcheix</i>	17
(Invited) Mn ₅ Ge ₃ C _{0.8} Contacts for Spin Injection Into Ge <i>I. A. Fischer, C. Sürgers, M. Petit, V. Le Thanh, J. Schulze</i>	29
(Invited) Development of Multifunctional Liner/Barrier Systems for Sub-14nm Metallization <i>E. Eisenbraun</i>	37
Optimization of Cu Damascene Electrodeposition Process in ULSI for Yield and Reliability Improvement <i>I. Shao, T. Cheng, P. Findeis, J. Kelly, S. Ahmed, M. Angyal, Y. Xu, B. Li, J. Tinkler, N. Lustig, E. Engbrecht, C. Truong, M. Chudzik, S. Grunow</i>	43

ALD W CMP for HKMG <i>T. Yang, G. Wang, Q. Xu, Y. Lu, J. Yu, H. Cui, J. Yan, J. Li, C. Zhao</i>	49
Fabrication of Metal-Nitride/Si Contacts with Low Electron Barrier Height <i>K. Yamamoto, K. Asakawa, D. Wang, H. Nakashima</i>	53

Chapter 3 Single Electron, Tunneling and Quantum Devices

(Invited) Single Electron and Single Atom CMOS Perspectives <i>X. Jehl, M. Sanquer, M. Vinet, R. Wacquez</i>	63
(Invited) High-Speed Operation of Si Single-Electron Transistor <i>Y. Takahashi, H. Takenaka, T. Uchida, M. Arita, A. Fujiwara, H. Inokawa</i>	73
(Invited) Si/SiGe Resonant Interband Tunnel Diodes Grown by Large-Area Chemical Vapor Deposition <i>P. Berger, A. Ramesh, R. Loo</i>	81
(Invited) Dopant-Atom-Based Tunnel SOI-MOSFETs <i>M. Tabe, D. Moraru, E. Hamid, A. Samanta, L. T. Anh, T. Mizuno, H. Mizuta</i>	89
(Invited) Wide Bandgap Heterojunctions on Crystalline Silicon <i>J. Sturm, S. Avasthi, K. Nagamatsu, J. Jhaveri, W. E. McClain, G. Man, A. Kahn, J. Schwartz, S. Wagner</i>	97

Chapter 4 Technology Trends

(Invited) Status and Future of IC Analog Technologies <i>A. Bergemont</i>	109
(Invited) MEMS and Photonics Module Integration into SiGe BiCMOS Technology for More than Moore Functional Diversification <i>B. Tillack, B. Heinemann, M. Kaynak, D. Knoll, S. Lischke, A. Mai, H. Rücker, Y. Yamamoto, L. Zimmermann</i>	115

(Invited) Bio-MEMS Chip for Bacteria Detection -A Challenge of Si Technology to Biomedical Field-	125
<i>H. Ishii, K. Sawada, M. Ishida, K. Machida, K. I. Iida, M. Saito, S. I. Yoshida</i>	

Chapter 5 Ge-based and III-V Technologies

(Invited) Performance Enhancement Technologies in III-V/Ge MOSFETs <i>S. Takagi, R. Zhang, S. H. Kim, M. Yokoyama, M. Takenaka</i>	137
(Invited) Heteroepitaxial Growth of Sn-Related Group-IV Materials on Si Platform for Microelectronic and Optoelectronic Applications: Challenges and Opportunities <i>O. Nakatsuka, N. Taoka, T. Asano, T. Yamaha, M. Kurosawa, M. Sakashita, S. Zaima</i>	149
(Invited) The Effect of Carbon Doping on Structural and Magnetic Properties of Mn ₅ Ge ₃ /Ge Heterostructures <i>A. Spiesser, M. T. Dau, L. A. Michez, M. Petit, V. Le Thanh</i>	157
(Invited) Development of Metal Source/Drain Ge-CMOS Using TiN/Ge and HfGe/Ge Contacts <i>H. Nakashima, K. Yamamoto, D. Wang</i>	167
High-Quality Hybrid-GeSn/Ge Stacked-Structures by Low-Temperature Sn Induced-Melting Growth <i>Y. Kinoshita, R. Matsumura, T. Sadoh, T. Nishimura, M. Miyao</i>	179
Characterization of Local Strain Structures in Heteroepitaxial Ge _{1-x} Sn _x /Ge Microstructures by Using Microdiffraction Method <i>S. Ike, Y. Moriyama, M. Kurosawa, N. Taoka, O. Nakatsuka, Y. Imai, S. Kimura, T. Tezuka, S. Zaima</i>	185

Chapter 6 Epitaxial Processing

(Invited) Group-IV Semiconductor Quantum Heterointegration by Low-Energy Plasma CVD Processing <i>M. Sakuraba, J. Murota</i>	195
---	-----

Atomically Flat Germanium (111) Surface by Hydrogen Annealing <i>T. Nishimura, S. Kabuyanagi, C. Lee, T. Yajima, K. Nagashio, A. Toriumi</i>	201
Formation and Characterization of Strained Si _{1-x} Ge _x Films Epitaxially Grown on Si(100) by Low-Energy ECR Ar Plasma CVD without Substrate Heating <i>N. Ueno, M. Sakuraba, J. Murota, S. Sato</i>	207
(Invited) Low-Temperature Metal-Induced Crystallization of Orientation-Controlled SiGe on Insulator for Flexible Electronics <i>T. Sadoh, J. H. Park, M. Kurosawa, M. Miyao</i>	213
Epitaxial Growth of Heavily B-Doped Si and Ge Films on Si(100) by Low-Energy ECR Ar Plasma CVD without Substrate Heating <i>Y. Abe, S. Kubota, M. Sakuraba, J. Murota, S. Sato</i>	223

Chapter 7 **Front-end Processing**

(Invited) Study on Charge Storage and Optical Response of Hybrid Nanodots Floating Gate MOS Devices for Their Optoelectronic Application <i>S. Miyazaki, M. Ikeda, K. Makihara</i>	231
Source and Drain Contact Module for FDSOI MOSFETs : Silicidation and Strain Engineering <i>V. Carron, F. Nemouchi, J. M. Hartmann, D. Cooper, J. F. Damlencourt, S. Bernasconi, S. Favier, Y. Morand</i>	239
Fin Doping by Hot Implant for 14nm FinFET Technology and Beyond <i>B. S. Wood, F. A. Khaja, B. P. Colombeau, S. Sun, A. Waite, M. Jin, H. Chen, O. Chan, T. Thanigaivelan, N. Pradhan, H. J. L. Gossman, S. Sharma, V. R. Chavva, M. P. Cai, M. Okazaki, S. S. Munnangi, C. N. Ni, W. Suen, C. P. Chang, A. Mayur, N. Variam, A. D. Brand</i>	249
Liquid-Solid Coexisting Annealing of a-GeSn/Si(100) Structure for Low Temperature Epitaxial Growth of SiGe <i>H. Chikita, R. Matsumura, T. Sadoh, M. Miyao</i>	257

Chapter 8

Device Characterization

(Invited) Characterization of Oxide Traps Participating in Random Telegraph Noise Using Charging History Effects in Nano-Scaled MOSFETs <i>T. Tsuchiya, N. Tamura, A. Sakakidani, K. Sonoda, M. Kamei, S. Yamakawa, S. Kuwabara</i>	265
Low-Frequency-Noise-Based Oxide Trap Profiling in Replacement High-k/Metal-Gate pMOSFETs <i>E. R. Simoen, J. W. Lee, A. Veloso, V. Paraschiv, N. Horiguchi, C. Claeys</i>	281
Resistive Switching Properties of $\text{SiO}_x/\text{TiO}_2$ Multi-Stack in Ti-Electrode MIM Diodes <i>A. Ohta, K. Makihara, M. Fukushima, H. Murakami, S. Higashi, S. Miyazaki</i>	293
Reduction of Interface States Density Due to Post Oxidation with Formation of AlGeO Layer at $\text{Al}_2\text{O}_3/\text{Ge}$ Interface <i>S. Shibayama, K. Kato, M. Sakashita, W. Takeuchi, N. Taoka, O. Nakatsuka, S. Zaima</i>	301
High Electron Mobility in Germanium Junctionless n-MOSFETs <i>S. Kabuyanagi, T. Nishimura, K. Nagashio, A. Toriumi</i>	309
Author Index	317