

2012 International Symposium on VLSI Design, Automation and Test

(VLSI-DAT 2012)

Hsinchu, Taiwan
23 – 25 April 2012



IEEE Catalog Number: CFP12847-PRT
ISBN: 978-1-4577-2080-2

TABLE OF CONTENTS

JOINT PLENARY SESSION

Advances in Computing	1
<i>Y. Zhang</i>	
Gaining 10x In Energy Efficiency In The Next Decade In Consumer Products.....	2
<i>P. Magarshack, A. Cathelin</i>	

JOINT SESSION I: SMART HANDHELD PLATFORM (ALL INVITED TALKS)

Powerful Smartphone Solutions Unleashing New Technology Innovations	4
<i>G. Huang</i>	
Disruptive Technologies for the Future Generation Smart Systems	5
<i>P. Lemmens</i>	
The 2012 ARM Powered Compute Subsystem – Delivering the Smart Handheld Platform.....	6
<i>T. Whitfield</i>	
Google's C/C++ Toolchain For Smart Handheld Devices.....	7
<i>D. Kwan, J. Yu, B. Janakiraman</i>	
Emerging Touch Techniques In Smart Handheld Device	11
<i>L. Lin, W. Chien</i>	

SPECIAL SESSION I: HIGH-POWER GREEN ELECTRONICS (ALL INVITED TALKS)

Silicon Carbide Devices Open a New Era of Power Electronics	13
<i>H. Takasu</i>	
Power Semiconductor - Driving Technology for High Power Green Electronic Systems	15
<i>L. Lorenz</i>	
Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array	17
<i>M. Tsai, Y. Lin, H. Yang, M. Tu, W. Shih, N. Lien, K. Lee, S. Jou, C. Chuang, W. Hwang</i>	
A 2kb Built-In Row-Controlled Dynamic Voltage Scaling Near-/Sub-Threshold FIFO Memory for WBANs.....	21
<i>W. Du, P. Huang, M. Chang, W. Hwang</i>	
An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array.....	25
<i>Y. Lin, M. Tsai, H. Yang, G. Lin, S. Wang, C. Chuang, S. Jou, W. Hwang, N. Lien, K. Lee, W. Shih</i>	
A Slew Rate Self-Adjusting 2×VDD Output Buffer With PVT Compensation	29
<i>C. Chen, H. Tseng, R. Kuo, C. Wang</i>	

SESSION M2: ADC/DAC

A 6b, 1GS/s, 9.9mW Interpolated Subranging ADC in 65nm CMOS	33
<i>T. Danjo, M. Yoshioka, M. Isogai, M. Hoshino, S. Tsukamoto</i>	
A 9-bit 100MS/s Tri-level Charge Redistribution SAR ADC with Asymmetric CDAC Array.....	37
<i>X. Zhu, Y. Chen, S. Tsukamoto, T. Kuroda</i>	
A 10-bit 200-MS/s Reconfigurable Pipelined A/D Converter.....	41
<i>C. Ho, T. Lee</i>	
A 14-bit 200MS/s Current-Steering DAC Achieving over 82dB SFDR with Digitally-Assisted Calibration and Dynamic Matching Techniques	45
<i>J. Tsai, Y. Chen, Y. Lai, M. Shen, P. Huang</i>	

VLSI-DAT PLENARY SESSION I

Ambient Electronics and Ultra-Low Power LSI Design.....	49
<i>T. Sakurai</i>	

SESSION T1: HARDWARE ARCHITECTURE OF MULTIMEDIA SYSTEMS

Low Bandwidth HD1080@60FPS JPEG-XR Transform Design	80
<i>S. Fan, J. Chen, J. Guo</i>	
A Lossless Embedded Compression Codec Engine for HD Video Decoding	84
<i>L. Chiu, T. Chang</i>	
Hardware-Efficient True Motion Estimator Based on Markov Random Field Motion Vector Correction	88
<i>F. Chen, Y. Huang, S. Chien</i>	

SESSION T2: MIXED-SIGNAL TECHNIQUES

Intel® Core™ i5/i7 QuickPath Interconnect Receiver Clocking Circuits and Training Algorithm.....	92
<i>N. Chowdhary, J. Wight, C. Mozak, N. Kurd</i>	
Time-Delay Integration Readout with Adjacent Pixel Signal Transfer for CMOS Image Sensor.....	96
<i>K. Cheng, C. Yin, C. Hsieh, W. Chang, H. Tsai, C. Chiu</i>	
A Fast-Locking Phase-Locked Loop Using CP Control and Gated VCO	100
<i>I. Lee, Y. Tsai, S. Liu</i>	

SESSION T3: EFFICIENT CHANNEL CODEC DESIGN

A Fully-Parallel Step-by-Step BCH Decoder over Composite Field for NOR Flash Memories.....	104
<i>Y. Chen, C. Yang, H. Chang</i>	
Efficient Architecture for Reed-Solomon Decoder	108
<i>Y. Lu, M. Shieh</i>	
Large Set Construction of User Uplink Ranging Codes for M2M Applications	112
<i>X. Wang, H. Ma, J. Hsu, P. Ting</i>	

SESSION T4: ANALOG TECHNIQUES

A 4.9-mW 4-Gb/s Single-to-Differential TIA with Current-Amplifying Regulated Cascode.....	116
<i>T. Lu, H. Lee, C. Wang</i>	
New Design on 2×VDD-Tolerant Power-Rail ESD Clamp Circuit with Low Standby Leakage in 65nm CMOS Process	120
<i>C. Yeh, M. Ker</i>	
40MHz Gm-C Filter with High Linearity OTA for Wireless Applications.....	124
<i>S. Hsu, C. Lu, C. Hung</i>	

SPECIAL LUNCH TALK

The Evolution of Fabless IC Industry in China: Past, Present, and Future	128
<i>P. Ko, P. Yue</i>	

JOINT SESSION II: NEW MEMORY SYSTEM (ALL INVITED TALKS)

Transforming Memory Systems: Optimizing for Client Value on Emerging Workloads	129
<i>K. Nowka</i>	
Emerging Memory Technology Perspective	131
<i>R. Bez, P. Cappelletti</i>	
Review of 3D High Density Storage Class Memory (SCM) Architecture	133
<i>B. Lee</i>	

Computer Architecture for Die Stacking.....	134
<i>G. Loh</i>	

SESSION T5: SOC DESIGN

Design of a Real-time Software-Based GPS Baseband Receiver Using GPU Acceleration	136
<i>J. Wu, L. Chen, T. Chiueh</i>	
Universal Architecture Prototype for Patient-Centric Medical Environment	140
<i>Y. Chenwu, H. Ma, C. Biswas, D. Markovic</i>	
An Efficient Memory Controller for 3D Heterogeneous Integration Platform	144
<i>Y. Liu, C. Yang, S. Chen, C. Chiu, C. Chu, C. Wu, C. Huang</i>	
Design and Implementation of 18-band Quasi-ANSI S1.11 1/3-Octave Filter.....	148
<i>C. Lin, K. Chang, M. Chuang, C. Liu</i>	

SESSION T6: TESTING AND FAULT-TOLERANT TECHNIQUES

3D-IC BISR for Stacked Memories Using Cross-die Spares.....	152
<i>C. Chi, Y. Chou, D. Kwai, Y. Hsiao, C. Wu, Y. Hsing, L. Deng, T. Lin</i>	
Routing-Efficient Implementation of An Internal-Response-Based BIST Architecture	156
<i>W. Lien, T. Hsieh, K. Lee</i>	
Statistical SDFC:A Metric for Evaluating Test Quality of Small Delay Faults.....	160
<i>X. Zhu, H. Li, X. Li</i>	
A Fault-Tolerant PE Array Based Matrix Multiplier Design	164
<i>B. Yan, J. Huang</i>	

SESSION T7: SOC DESIGN METHODOLOGY

IMITATOR: A Deterministic Multicore Replay System with Refining Techniques	168
<i>S. Chen, C. Wen, G. Yang, W. Jone, T. Chen</i>	
Transport-Layer Assisted Vertical Traffic Balanced Routing for Thermal-Aware Three-Dimensional Network-on-Chip Systems	172
<i>K. Chen, C. Chao, S. Lin, H. Hung, A. Wu</i>	
A Power Management Technology for Mobile Embedded System.....	176
<i>S. Wen, C. Chen, S. Tung</i>	
A Highly Parallel Design of Image Surface Layout Recovering on GPGPU	180
<i>G. Li, B. Lai</i>	

SESSION T8: ADVANCED PERFORMANCE-DRIVEN DESIGN OPTIMIZATION

Peak Wake-up Current Estimation at Gate-level with Standard Library Information	184
<i>M. Lee, Y. Liu, W. Wu, C. Liu</i>	
A Nonlinear Optimization Methodology for Resistor Matching in Analog Integrated Circuits	188
<i>S. Jiang, C. Wu, T. Ho</i>	
3-D Centric Technology and Realization with TSV	192
<i>C. Lin, C. Lee, T. Tseng, D. Kwai, Y. Chou</i>	

SESSION T9: ALL-DIGITAL CLOCK CIRCUITS

A Low-Power and Small-Area All-Digital Spread-Spectrum Clock Generator in 65nm CMOS Technology	196
<i>C. Chung, D. Sheng, W. Ho</i>	
Cyclic-MPCG : Process-Resilient and Super-Resolution Multi-Phase Clock Generation by Exploiting the Cyclic Property	200
<i>R. Ding, S. Huang, C. Tzeng, S. Fang, C. Weng</i>	
A Range Extending Delay-Recycled Clock Skew-Compensation And/Or Duty-Cycle-Correction Circuit.....	204
<i>S. Wei, Y. Wang, J. Peng, Y. Surya</i>	

A High-Speed Dual-Phase Processing Pipelined Domino Circuit Design with a Built-in Performance Adjusting Mechanism.....	208
<i>C. Cheng, J. Guo</i>	

SESSION T10: HIGH LEVEL SYNTHESIS AND ROBUST DESIGN METHODOLOGY

Port Assignment for Interconnect Reduction in High-Level Synthesis	212
<i>H. Cong, S. Chen, T. Yoshimura</i>	
ASIC Synthesis using Architecture Description Language.....	216
<i>Z. Wang, X. Wang, A. Chattopadhyay, Z. Rakosi</i>	
Design Validation on Multiple-Core CPU Supported Low Power States Using Platform Based Infrared Emission Microscopy (PIREM) Technique.....	220
<i>Y. Chen, D. Budka, A. Gibertini, D. Bockelman, Y. Lin</i>	
Spatial-Correlation-Aware Soft Error Rate Analysis using Quasi-importance Sampling	224
<i>X. Wu, K. Hsu, L. Chang, C. Wen</i>	

INDUSTRY SESSION I: STATE-OF-THE-ART SOC DESIGN AND PLATFORM

A 363-μW/fps Power-Aware Green Multimedia Processor for Mobile Applications	228
<i>C. Ju, Y. Chang, C. Wang, C. Chen, H. Lin, C. Cheng, S. Wang, T. Liu, C. Tsai</i>	
High Speed DDR2/3 PHY and Dual CPU Core Design for 28nm SoC.....	232
<i>K. Ho, T. Chou, P. Chen, D. Liou</i>	
The Best SoC Solution with AndesCore and Andes's Platform.....	237
<i>S. Jiang, F. Iin</i>	

INDUSTRY SESSION II: ADVANCED SOC/3D-IC DESIGN METHODOLOGY

Test for More Than Pass/Fail Using On-chip Temperature Sensor	241
<i>C. Wang, C. Lin, C. Hsu, C. Wu</i>	
A Novel Design Methodology for Hybrid Process 3D-IC	245
<i>C. Huang, N. Chang, C. Chen, C. Lin, C. Wu, C. Huang</i>	
Challenges and Solutions in Modern Analog Placement	249
<i>T. Chen, T. Kuan, C. Hsieh, C. Peng</i>	

PLENARY SESSION II

Technology and Design Challenges for Smartphone SOCs.....	253
<i>K. Loh</i>	

SPECIAL SESSION II: DESIGN METHODOLOGY FOR ADVANCED TECHNOLOGIES

Data Mining Based Prediction Paradigm and Its Applications in Design Automation	254
<i>M. Abadir, N. Sumikawa, W. Chen, L. Wang</i>	
VLSI CAD for Emerging Nanolithography.....	255
<i>D. Pan, J. Gao, B. Yu</i>	
Area and Reliability Efficient ECC Scheme for 3D RAMs	259
<i>L. Chang, Y. Huang, J. Li</i>	

SESSION W1: POWER CONVERSION TECHNIQUES

An Area-Efficient CMOS Switching Converter with On-Chip LC Filter Using Feedforward Ripple Cancellation Technique	263
<i>P. Lan, Y. Kuo, P. Huang</i>	
On Investigation into A CMOS-process-based High-voltage Driver Applied to Implantable Microsystem	267
<i>C. Gong, K. Yao, J. Hong, M. Shiu</i>	

Wireless Power Link Design Using Silicon-Embedded Inductors for Brain-Machine Interface	271
<i>R. Wu, S. Raju, M. Chan, J. Sin, C. Yue</i>	

SESSION W2: POWER AMPLIFIER AND ENERGY-EFFICIENT TRANSMITTER

A Monolithic 1.85GHz 2-Stage SiGe Power Amplifier with Envelope Tracking for Improved Linear Power and Efficiency.....	275
<i>R. Wu, Y. Li, J. Lopez, D. Lie</i>	
Variable Gain Active Predistorter with Linearity Enhancement for a 2.4 GHz SiGe HBT Power Amplifier Design.....	279
<i>K. Lin, H. Chiou, P. Wu, C. Sha, C. Ko, D. Chang, Y. Juang</i>	
An Energy-Efficient Ultra-Wideband Transmitter with an FIR Pulse-Shaping Filter	283
<i>W. Liu, T. Lin</i>	

POSTER SESSION

A 1-V 60 GHz CMOS Low Noise Amplifier with Low Loss Microstrip Lines	287
<i>C. Ko, C. Chang, C. Kuo, D. Chang, Y. Juang</i>	
A 1-V, 44.6 ppm/$^{\circ}$C Bandgap Reference with CDS Technique.....	291
<i>P. Chen, S. Chang, C. Huang, C. Lin</i>	
A Highly Integrated Class-D Amplifier using Driver Delay Hysteresis Control	295
<i>J. Tai, H. Chen, H. Chiu</i>	
A Low-Power, Capacitively-Divided, Ring Oscillator with Digitally Adjustable Voltage Swing.....	299
<i>T. Jiang, P. Chiang, K. Hu</i>	
An Energy-Saving Spectrum Sensing Processor Based on Partial Discrete Wavelet Packet Transform.....	303
<i>C. Yang, C. Hsieh, Y. Huang</i>	
DVB-T2 LDPC Decoder with Perfect Conflict Resolution.....	307
<i>X. Zhao, Z. Chen, X. Peng, D. Zhou, S. Goto</i>	
A Low Cost DPA-Resistant 8-bit AES Core Based on Ring Oscillators.....	311
<i>H. Fu, J. Hsiao, P. Liu, H. Chang, C. Lee</i>	
A Hardware In The Loop Design Methodology For FPGA System And Its Application To Complex Functions	315
<i>G. Liang, D. He, J. Portilla, T. Riesgo</i>	
Design and Implementation of an Optical OFDM Baseband Receiver in FPGA	319
<i>Y. Hwang, S. Tsai, Y. Chen</i>	
An OCP-AHB Bus Wrapper with Built-in ICE Support for SOC Integration	323
<i>C. Wu, F. Huang, K. Kuo, I. Huang</i>	
Design of a Pipelined Clos Network with Late Release Scheme.....	327
<i>W. Tang, Y. Hsu</i>	
Performance Validation of Dynamic-Remapping-Based Task Scheduling on 3D Multi-Core Processors.....	331
<i>C. Liao, H. Wen</i>	
A Master-Slave SoC Structure for HMM Based Speech Recognition.....	335
<i>H. Geng, Y. Shi, M. Dong, R. Liu</i>	
Post-Bond Test Techniques for TSVs with Crosstalk Faults in 3D ICs	339
<i>Y. Huang, J. Li, C. Chou</i>	
3D IC Test Scheduling Using Simulated Annealing.....	343
<i>C. Hsu, C. Kuo, J. Li, K. Chakrabarty</i>	
Author Index	