Proceedings

12 IEEE EUROPEAN TEST SYMPOSIUM

ETS 2007

TABLE OF CONTENTS

ETS 2007

Foreword ... ix

Organizing Committee ... x

Steering Committee ... xii

Program Committee ... xii

ETS 2006 Paper Award ... xiii

Test Technology Technical Council ... xiv

Plenary Presentations

If It's All about Yield, Why Talk about Testing? ... 3
René Segers

Electronics Design-for-Test: Past, Present and Future ... 4
Ben Bennetts

Fault and Defect Diagnosis

Adaptive Debug and Diagnosis without Fault Dictionaries ... 7
Stefan Holst and Hans-Joachim Wunderlich

DERRIC: A Tool for Unified Logic Diagnosis ... 13
A. Rousset, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, and A. Virazel

Mixed Signal DFT and Test

A Digitally Testable Capacitance-Insensitive Mixed-Signal Filter ... 21
Erik Schüler, Marcelo Negreiros, Pascal Nouet, and Luigi Carro

NoC Testing

Test Configurations for Diagnosing Faulty Links in NoC Switches 29
Jaan Raik, Raimund Ubar, and Vineeth Govind

Optimization of NoC Wrapper Design under Bandwidth and Test Time Constraints 35
Fawnizu Azmadi Hussin, Tomokazu Yoneda, and Hideo Fujiwara

Advances in RF Test

FPGA Architecture for RF Transceiver System and Mixed-Signal Low Cost Tests 43
Ivo Koren, Frank Demmerle, Roland May, Martin Kaibel, and Sebastian Sattler

Digital Generation of Signals for Low Cost RF BIST 49
Marcelo Negreiros, Luigi Carro, and Altamiro A. Susin

Variance Reduction for Supply Ramp Based Cheap RF Test Alternatives 55
Shaji Krishnan, René Jonker, and Leon van de Logt

Diagnosis and Debug

Parallel Scan-Like Testing and Fault Diagnosis Techniques for Digital Microfluidic Biochips 63
Tao Xu and Krishnendu Chakrabarty

Communication-Centric SoC Debug Using Transactions 69
Bart Vermeulen, Kees Goossens, Remco van Steeden, and Martijn Bennebroek

Simulation and Verification

Electrical Simulation Model of the 2T-FLOTOX Core-Cell for Defect Injection
and Faulty Behavior Prediction in eFlash Memories 77
O. Ginez, J.-M. Daga, P. Girard, C. Landrault, S. Pravossoudovitch, and A. Virazel

Memory Test

PPM Reduction on Embedded Memories in System on Chip 85
Said Hamdioui, Zaid Al-Ars, Javier Jimenez, and Jose Calero

An Integrated Built-in Test and Repair Approach for Memories with 2D Redundancy 91
Philipp Öhler, Sybille Hellebrand, and Hans-Joachim Wunderlich

Dynamic Two-Cell Incorrect Read Fault due to Resistive-Open Defects
in the Sense Amplifiers of SRAMs 97
A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, and M. Bastian

On-Line Testing and Self-Test

A Novel Approach for Online Sensor Testing Based on an Encoded Test Stimulus 105
N. Dumas, Z. Xu, K. Georgopoulos, J.F.T. Bunyan, and A. Richardson

Selecting Power-Optimal SBST Routines for On-Line Processor Testing 111
A. Merentitis, N. Kranitis, A. Paschalis, and D. Gizopoulos

Optimal Contexts for the Self-Test of Coarse Grain Dynamically Reconfigurable Processors 117
Tomoo Inoue, Takashi Fujii, and Hideyuki Ichihara

Fault Grading and Test Quality

A Seed-Selection Method to Increase Defect Coverage for LFSR-Reseeding-Based Test Compression 125
Zhanglei Wang, Krishnendu Chakrabarty, and Michael Bienek

Ultra Fast Parallel Fault Analysis on Structurally Synthesized BDDs 131
Raimund Ubar, Sergei Devadze, Jaan Raik, and Artur Jutman

Computation and Application of Absolute Dominators in Industrial Designs 137
René Krenz-Bååth, Andreas Glowatz, and Juergen Schloeffel

Diagnosis and Yield Improvement

Analyzing Volume Diagnosis Results with Statistical Learning for Yield Improvement 145
Huaxing Tang, Sharma Manish, Janusz Rajski, Martin Keim, and Brady Benware

Diagnostic Test Generation Based on Subsets of Faults 151
Irith Pomeranz and Sudhakar M. Reddy

Single Event Upsets

Static and Dynamic Analysis of SEU Effects in SRAM-Based FPGAs 159
L. Sterpone and M. Violante

System Level Approaches for Mitigation of Long Duration Transient Faults in Future Technologies 165
C.A. Lisbôa, M.I. Erigson, and L. Carro

Delay and Performance Test

Automatic Generation of Instructions to Robustly Test Delay Defects in Processors 173
Sankar Gurumurthy, Ramtilak Vemu, Jacob A. Abraham, and Daniel G. Saab

On the Automatic Generation of Test Programs for Path-Delay Faults in Microprocessor Cores 179
P. Bernardi, M. Grosso, E. Sánchez, and M. Sonza Reorda

Purely Digital BIST for Any PLL or DLL 185
Stephen Sunter and Aubin Roy

Embedded Tutorials

System-in-Package, A Combination of Challenges and Solutions 193
P. Cauvet, S. Bernard, and M. Renovell

Embedded Tutorial: IC Test Cost Benchmarking 200
Klaus Luther

Wafer Level Reliability Screens 201
Peter Maxwell

Embedded Tutorial on Low Power Test 202
Nicola Nicolici and Xiaoqing Wen

ETS06 Best Paper

"Analogue Network of Converters": A DFT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SOC 211
V. Kerzérho, P. Cauvet, S. Bernard, F. Azaïs, M. Comte, and M. Renovell

Author Index 217